OPERA

LOw Power Heterogeneous Architecture
for NExt Generation of SmaRt Infrastructure and Platforms
in Industrial and Societal Applications

Dissemination – Report 2

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EXECUTIVE SUMMARY

This document---the second dissemination report---describes the dissemination efforts that were carried out in the 10 months (M17—M26) that passed since the first dissemination report (deliverable 8.8, which was submitted in M16 of the OPERA project). This deliverable gives a thorough account of all OPERA activities that were carried out by all partners to distribute information to various audiences within the academic and industrial communities.

Following the recommendations of the second review report, we also enhance and broaden the original dissemination plan (deliverable 8.4, which was submitted in M4 of the OPERA project). First, we describe and elaborate which conferences or journals from the exhaustive lists will be targeted in the third (and last) year of the OPERA project.

Second, we describe three journal papers that the OPERA consortium is planning to publish in the last year of the project. These three papers will add to the overall goal of six published papers, which was set in the original dissemination plan. We believe that increasing the number of scientific publications will address a major concern of the reviewers regarding the OPERA dissemination plan, as was raised by the commission in the second review (held in Brussels on 20 July 2017).

The OPERA consortium also enhanced the dissemination activities through the active participation in the events organised by HiPEAC (the main HiPEAC conference, the Computing System Weeks (CSW), the sponsored booth on international conferences). HiPEAC is a well-established community comprising academic, centers of excellence, and industrial members in the domain of high-performance, low-power computer architecture and design (covering both the software and hardware aspects). Attending the HiPEAC events allowed OPERA to create important connections with other Horizon 2020 projects, as well as to share project results.

Position of the deliverable in the whole project context

Dissemination is essential for the success of the project and for the sustainability of outputs in the long term. This report (D8.12), as well as the previous D8.8 and the final D8.14, are all periodical reports of the activities aimed at fulfilling the OPERA dissemination plan, which was described in D8.4. Importantly, D8.4 set clear and measurable targets to monitor and report the outcomes of the project.

This intermediate report is important because it demonstrates that the OPERA project is following well the plan that we set in D8.4 and is in some cases exceeding the targets. We expect that when the project will reach its final stages, the OPERA consortium will meet all its dissemination goals by publishing more papers and organizing more events and workshops. We therefore believe that thousands of scientists and engineers will be reached and learn from the OPERA project.

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1 DISSEMINATION PROGRESS

The OPERA dissemination plan, which was already submitted under Deliverable 8.4 (D8.4), was significantly enhanced. Table 1 presents the original dissemination plan and the improved plan. The main improvement was to increase the OPERA target for scientific publications from six to nine, according to the comments of the reviewers in the second review (held in Brussels on 20 July 2017):

"The consortium is requested for the next version of this report (D8.12) to revise the planned number of published papers… It is currently too low for a project of this size, duration and ambition. "

Henceforth, we will only describe the enhanced OPERA dissemination plan. The overall strategy of dissemination, defined by all the partners for communicating their OPERA research results throughout the project, has not changed. We measure the progress of our dissemination with clear and quantitative targets so as to allow monitoring and reporting the outcomes:

Target #1: publish 9 papers along the OPERA project in total, such that each academic or research partner (Technion, ISMB, IBM) is involved in at least 3 of these papers.

Target #2: reach 4,000 people from the academic community in total. In other words, we want that at least 2,000 researchers will attend the conferences where OPERA works were presented or will read the journals where OPERA works were published.

Target #3: write at least one report for every task.

Target #4: organize 10 workshops/events along the OPERA project in total, one per industrial partner (Certios, HPE, Nallatech, Neavia, ST, Teseo).

The following sections describe the status of each of the targets, and Table 1 summarizes the progress made so far. Overall, the pace of the progress is satisfactory and sometimes even better than expected, e.g., for Targets #2, #4. Note that this document gives only an intermediate report, and so we should not expect to entirely fulfill all the targets yet. We expect that in the third year of the project we will reach our targets.

Table 1: Progress of the dissemination targets

	Original Plan D8.4	Last report (M16)	**Improved Plan D8.12**	**Current (M26)**	**Progress ratio**
Target #1 (published papers)	6	3	**9**	**7**	**78%**
Target #2 (researchers reached)	2,000	2,000	**4,000**	**3,000**	**75%**
Target #3 (reports per task)	1	1	**1**	**1**	**100%**
Target #4 (events/workshops)	6	3	**10**	**9**	**90%**

1.1 STATUS OF TARGET #1

The academic partners of OPERA (Technion, ISMB, and IBM) have published four new papers in the second period of the project (M16—M26), as described below. These papers (and the posters we used

to present these works) were also published in the OPERA website, the OPERA Facebook page, and the OPERA Twitter page.

1.1.1 Paper #1: Remote page faults with a CAPI based FPGA

Authors: Nider, J., Binyamini, Y., Rapoport, M.

Title: "Remote page faults with a CAPI based FPGA"

Venue: SYSTOR '17 Proceedings of the 10th ACM International Systems and Storage Conference

Date: May 22 – 24, 2017

Location: Haifa, Israel

DOI: https://doi.org/10.1145/3078468.3078489

Abstract:

Post-copy VM or container migration requires that the bulk of the memory is transferred after resuming on the destination node. Transferring memory between nodes over a commodity TCP/IP network incurs too much latency, which slows down execution of the application on the destination node.

1.1.2 Paper #2: User space memory management for post-copy migration

Authors: Rapoport, M., Nider, J.

Title: "User space memory management for post-copy migration"

Venue: SYSTOR '17 Proceedings of the 10th ACM International Systems and Storage Conference

Date: May 22 – 24, 2017

Location: Haifa, Israel

DOI: https://doi.org/10.1145/3078468.3078490

Abstract:

Post-copy migration allows reduction of application down-time and reduces overall network bandwidth used for application migration. Migration can be used to help optimize several aspects of operations such as power efficiency. The userfault technology recently introduced to the Linux kernel allows post-copy migration of virtual machines. However, this technology is missing essential features required for post-copy migration of Linux containers.

1.1.3 Paper #3: Systems Software for Fast Inter-Machine Page Faults

Authors: Nider, J., Rapoport, M., Binjamini, Y.

Title: Systems Software for Fast Inter-Machine Page Faults

Venue: Future Technologies Conference 2017

Date: November 29-30, 2017

Location: Vancouver, Canada

DOI: the paper is still not available online

Abstract:

Cloud computing abstracts the underlying hardware details from the user. As long as the customer Service Level Agreements (SLA) are satisfied, cloud providers and operators are free to make infrastructural decisions to optimize business objectives, such as operational efficiency of cloud data centers. By adopting a holistic view of the data center and treating it as a single system, a cloud provider can migrate application components and virtual machines within the system according to policies such as load balancing and power consumption. We contribute to this vision by removing architectural barriers for workload migration and reducing the downtime of migrating processes. We combine the post-copy approach to workload migration with a novel specialized low latency interconnect for handling resulting remote page faults. In this work, we introduce a cross-architecture workload migration system, specify the requirements towards the specialized interconnect, discuss design trade-offs and issues, and present our proposed SW-HW co-design.

1.1.4 Paper #4: Open-source implementation of an Ad-hoc IEEE 802.11 a/g/p software-defined radio on low-power and low-cost general purpose processors

Authors: Ciccia, S., G. Giordanengo, and G. Vecchi.

Title: “Open-source implementation of an Ad-hoc IEEE 802.11 a/g/p software-defined radio on low-power and low-cost general purpose processors”.

Publication Type: journal article.

Venue: Radioengineering, volume 26, number 4, pages 1083—1095.

Date: December 2017.

DOI: http://dx.doi.org/10.13164/re.2017.1083

Abstract:

This work proposes a low-cost and low-power software-defined radio open-source platform with IEEE 802.11 a/g/p wireless communication capability. A state-of-the-art version of the IEEE 802.11 a/g/p software for GNU Radio (a free and open-source software development framework) is available online, but we show here that its computational complexity prevents operations in low-power general purpose processors, even at throughputs below the standard. We therefore propose an evolution of this software that achieves a faster and lighter IEEE 802.11 a/g/p transmitter and receiver, suitable for low-power general purpose processors, for which GNU Radio provides very limited support; we discuss and describe the software radio processing structuring that is necessary to achieve the goal, providing a review of signal processing techniques. In particular, we emphasize the advanced reduced-instruction set (RISC) machine (ARM) study case, for which we also optimize some of the processing libraries. The presented software will remain open-source.

1.2 STATUS OF TARGET #2

According to the communication reports filled by all OPERA partners, the estimated number of researchers who were exposed to the OPERA findings and products in the first period of the project (M1—M16) is 2,000. Some of these are scientists and engineers who attended the conferences where OPERA works were presented or read the journals where OPERA works were published. Other researchers have heard about the OPERA innovative plans and products through presentations and posters delivered by the OPERA partners. We list some of these dissemination activities below:

- ISMB: SC17 (SuperComputing, Denver US), November 2017.

- Nallatech: SC17 (SuperComputing, Denver US), November 2017. The world's premier conference for all things high performance computing. Nallatech regularly attend this conference to present updates to customers and industrial partners. This year a representative of the OPERA project attended to disseminate the work done on the OPERA project regarding the FPGA compute acceleration. This a larger conference with over 10,000 delegates.
- Nallatech: ISC (International supercomputing), June 2017 in Frankfurt. An update of the OPERA project has discussed with academics and industrial partners at this conference, with engineering samples available to inspect.
- Nallatech: Computing Insight, December 2017. A presentation of FPGA acceleration was presented using the CNN offload activities of OPERA as an example.
- Nallatech: Internal OPERA workshop on FPGA programming with OpenCL (part 1, November 2017, Bristol UK).
- Nallatech: Internal OPERA workshop on FPGA programming with OpenCL (part 2, January 2018, Grenoble FR).
- Certios: IT Room infra (Den Bosch, 2017), participating in energy efficiency and datacenters event. Interacting with industry and academics.
- Certios: Ireland DC Conference (Dublin, 2017), workshop on the energy efficiency of the procurement process of IT infrastructure for public organizations. Explained the objectives of OPERA to small audience.
- Certios: DCW Frankfurt (Frankfurt, 2017), presented different models for energy efficiency and how to make these applicable in datacenters. Inspired by the conference and the excellent speakers. Interacting with industry and academics.
- IBM: Mike Rapoport (together with Reber A.) had a talk titled "Lazy process migration" [1] in the Linux Plumbers Conference 2016, which held on November 1-4, Santa Fe, New Mexico, USA.
- TESEO: ITS European Congress 2017, 19-22 June - Strasbourg
- TESEO: European Night of Researchers 2017, 29th September – Turin

1.3 STATUS OF TARGET #3

In the original OPERA grant agreement, all OPERA tasks committed to deliver one document that summarizes the work under this task. According to the feedback from the reviewers in the first review (M9), most of the tasks further committed to one or more intermediate reports and deliverables, thus enhancing and promising the achievement of Target #3. Moreover, all OPERA deliverables so far were delivered on time.

1.4 STATUS OF TARGET #4

In the second period (M16—M26) of the OPERA project, ISMB organized several workshops and events in which they presented OPERA results. These events were hosted under the HiPEAC ("High Performance and Embedded Architecture and Compilation") European network of excellence, which is one of the most active research communities in the computer architecture field, promoting several events and allowing EU projects to disseminate results and objectives.

Over the past few years, the HiPEAC network allows EU funded projects to become stakeholder members to better represent the project in front of the community and allows to share results, ideas and common objectives. The OPERA project is one of the stakeholders of the network [2] since November 2016, which enables to disseminate and spread the OPERA results effectively. There is also a HiPEAC conference organized every year, which is a good venue to meet other groups, and to search partners for collaborations. Similarly, HiPEAC also organizes twice a year a smaller event called

Computing System Week (CSW), where EU projects, academic and industrial partners can share their research results.

The HiPEAC membership, signed in 2016, allowed the OPERA consortium to be more effective in presenting the results of the research activity carried out to the academic and industrial community. Specifically, OPERA was present to the major events organized by the HiPEAC network of excellence, including the main conferences and the CSW. Specifically, during the latest CSW event held in November 2017 (Stuttgart, D), the OPERA consortium organised a thematic session titled “Heterogeneous and Low Power Architectures for the next Generation Cloud and Cyber-Physical Infrastructures”. This event allowed us to increase the dissemination of project results and activities, thanks to 4 scheduled presentations covering all the main challenges faced by OPERA and their related solutions. Also, other EU projects working in the domain touched by the Horizon 2020 – ICT4 call, as well as on high-performance and energy efficiency were represented. Specifically, DREDBOX, VINEYARD, M2DC, READEX, ANTAREX, and PHANTOM projects shared their results, thus facilitating reaching the goal of finding a common set of technologies to leverage on. During the event, more than 20 people were contacted (including people attending the thematic session and visiting the poster booth area).
The CSW event also served as the basis for the organization of the first workshop on the Heterogeneous and Low Power Data Center technologies held in Manchester during the main HiPEAC 2018 conference. This workshop allowed us to further expand the group of scientists and researchers reached by OPERA. The workshop offered the opportunity to present our latest results regarding architectural design, use of low power high performance technologies, as well as to encourage and foster the share of ideas with academic and industrial partners. Again, EU projects active in the research domain of the Horizon 2020 – ICT4 call were present, as well as important industrial and academic partners (e.g., ARM, BSC and IT4Innovations to mention few).
At both the events, OPERA was also present with a booth area with posters showing the technologies and solutions in the context of the three main use cases.

2 DISSEMINATION ROADMAP

As was previously mentioned, we improved and extended the original OPERA dissemination plan, which was submitted under D8.4, by increasing our dissemination targets. In this section, we outline the dissemination roadmap---the conferences and journals in which we will present the OPERA works---that will help us to meet the increased dissemination goals. The dissemination roadmap also addresses a major concern raised by the reviewers in the second review (held in Brussels on 20 July 2017):

"The deliverable [D8.4] should be updated such that it provides a clear commitment of the consortium, clearly showing which events the consortium plans to contribute to. "

2.1 CONFERENCES ROADMAP

Table 2 outlines the venues and conferences in which OPERA intends to publish its scientific findings. To avoid repetition, we only provide the venue name and its type; the venues are thoroughly described in D8.4 (the original dissemination plan).

Table 2: Conferences roadmap

Partner	Venue	Venue type	Plan
ISMB	HiPEAC 2018	Scientific conference	organize a workshop
	CISIS 2018	Scientific conference	present a paper
	SYSTOR 2018	Scientific conference	present a paper
	ISC 2018	Scientific and industrial event	present a poster/paper
TECHNION	ISCA 2018	The top four venues for computer architects	present a paper in one of the four
	MICRO 2018		
	ASPLOS 2018		
	HPCA 2018		
IBM	HiPEAC 2018	Scientific conference	present at the workshop organized by ISMB
	CLOUD 2018	Scientific conference	present a paper in one (or hopefully more) of these four venues
	SoCC 2018	Scientific conference	
	SYSTOR 2018	Scientific conference	
	OSDI 2018	Scientific conference	
TESEO	ITS 2018	Scientific conference	attend the event presenting the use case "Traffic Monitoring" at Eiffage Stand
	European Night of Researchers 2018	Scientific conference	Attend the event presenting OPERA project results in September 2018.

	HiPEAC 2018	Scientific conference	present at the workshop organized by ISMB
CERTIOS	URECA event (London, 2018)	Scientific and industrial event	organized together with UEL (University of East London). Webinars, workshops and presentations on IT energy efficiency.
	ISC-2018	Scientific and industrial event	present OPERA, participate in workshops
NALLATECH	HiPEAC 2018	Scientific conference	Presenting work regarding using FPGAs within Docker containers.
	HPE TSS (March 2018)	HPE event for internal and external partners	Presenting alongside HPE on AI inference referencing the CNN offload work underway for OPERA.
STM	HiPEAC 2018	Scientific conference	Presenting the Convolutional Neural Network System on Chip for Autonomous Intelligent Embedded Systems

2.2 JOURNALS ROADMAP

To further strengthen the OPERA dissemination plan, the OPERA consortium decided to carry out a joint effort and publish three journal papers that will comprehend the main OPERA technologies:

1. FPGA acceleration
2. Energy aware orchestration
3. ULP device in the computing continuum perspective

The three topics reported above involve the work done in the technical work packages (WP3, WP4, WP5 and WP6) and are also relevant to WP7 in terms of applications. Below we provide an initial organisation of the journal papers, and a preliminary distribution of the effort.

2.2.1 FPGA acceleration

Journal	IEEE Transactions on Sustainable Computing (TSUSC)
	Elsevier Microprocessors and Microsystems (MICPRO)
Topic	FPGA acceleration and energy efficiency enhancement

Title	TBD
Partner involved	ISMB, NALLATECH, HPE, CERTIOS

Section	**ISMB**	**NALL**	**HPE**	**CERT**
Abstract	X	X	X	X
1. Introduction	X			
1.1 Contribution	X			
2. Background (describing different use of FPGA in Cloud environment, such as catapult, memcache, AI, etc.)	X			X
3. Energy efficiency (discuss the model and methodology we use to evaluate the energy efficiency of the platform, in this case of the accelerator; here we reuse concepts and material from OPERA deliverable D4.1 and subsequents)		X	X	X
4. Acceleration system overview		X	X	
4.1 The FPGA device, board (considering HW parts, also with small description of the Intel-Altera device specific, ARM subsystem, etc.)		X	X	
4.2 Programming model and language (OpenCL and BSP)		X	X	
5. Experimental results (environment used to execute the experiments, simulation, baseline system -- only CPU, etc.)	X	X	X	X
5.1 Orthophoto correction acceleration (describe this use case; we also need to highlight the energy efficiency gain w.r.t. a baseline system -- only CPU, comparison with GPU acceleration ?)		X	X	
5.2 CNN acceleration of Caffe model ? (here it should be important and more critical to have some experimental data to compare with)		X		X
6. Conclusion	X	X	X	X
References	X	X	X	X

2.2.2 Energy aware orchestration

Journal	(Wiley) Concurrency and Computation: Practice and Experience (CCPE)
	IEEE Transactions on Sustainable Computing (TSUSC)
Topic	Orchestration and energy efficiency in data centers
Title	TBD
Partner involved	ISMB, IBM, TECNION, CERTIOS

Section	**ISMB**	**IBM**	**TECN**	**CERT**
Abstract	X	X	X	X
1. Introduction	X	X	X	X
1.1 Contribution	X	X	X	X
2. Background (describing heterogeneity in the data center, issues and challenges in managing large infrastructures, containerization, etc.)	X	X	X	X
3. Orchestration (describing in a more general fashion the concept)	X			
3.1 Containerization technology (what it is, advantages and disadvantages, microservice mapping, etc.)	X	X		
3.2 Technologies used to orchestrate containers in the data centers	X			
4. Energy efficiency (discuss the model and methodology we use to evaluate the energy efficiency of the whole data center, describe that two points are important to improve efficiency: using containers vs. traditional VMs, improving virtual memory support -- i.e., page walkthrough)			X	X
4.1 Introducing also the virtual memory subsystem improvements towards energy efficient orchestration/management			X	X
4.2 Container migration problem		X		X
5. Our system: introducing OPERA approach using a energy-aware microservice allocator, and container migration support across different architectures, etc.)	X	X		X

5.1 Description of the energy-aware resource allocator (both static and dynamic algorithm)	X			
5.2 Description of the container migration technology (how it works)		X		
5.3 Description of the virtual memory technology (hash-based page walkthrough)			X	
6. Conclusion	X	X	X	X
References	X	X	X	X

2.2.3 ULP device in the computing continuum perspective

Journal	Elsevier Microprocessors and Microsystems (MICPRO)
	IEEE Transactions on Sustainable Computing (TSUSC)
Topic	Making the edge of cloud energy efficient with ULP cyber-physical systems
Title	TBD
Partner involved	ISMB, STM, CERTIOS

Section	**ISMB**	**STM**	**CERT**
Abstract	X	X	X
1. Introduction (general positioning of the paper content, also referring to the OPERA project)	X		
1.1 Contribution	X		
2. Background (describing current CPS capabilities, architectures, acceleration function, power/energy efficiency)	X	X	
3. Energy efficiency in the context of ULP device and computing continuum			X
3. System overview (general description of the whole opera ULP system: camera, wireless communication front-end, acceleration function, energy harvesting, etc.)	X	X	X

3.1 ULP processor architecture description		X	
3.2 Wireless communication and reconfigurable antenna	X		
3.3 Acceleration function and CNN		X	
3.4 Energy harvesting			X
4. Experimental results (environment used to test, simulations, benchmark used, etc.)	X	X	
4.1 ULP processor performance (some data on some benchmark, e.g. using CNN or other benchmarks)		X	
4.2 Reconfigurable antenna and wireless front-end	X		
4.3 Energy efficiency analysis			X
6. Conclusion	X	X	X
References	X	X	X

3 CONCLUSIONS

First and foremost, this deliverable outlines the improved dissemination plan (compared to the original plan from deliverable 8.4, which was submitted in M4 of the OPERA project). The improved plan was devised according to the recommendations of the second review report, notably by increasing the number of scientific publications. To this end, we described three journal papers that the OPERA consortium is planning to publish in the last year of the project.

We then carefully reported the dissemination efforts that were carried out in the 10 months (M17—M26) that passed since the first dissemination report (deliverable 8.8, which was submitted in M16 of the OPERA project). We measured our progress according to the measurable targets that were set in the dissemination plan.

Last, we described the HiPEAC-related events that we organised by the OPERA consortium to ensure that the project results will be distributed to various audiences within the European academic and research-oriented community. HiPEAC is a well-established community comprising academic, centers of excellence, and industrial members in the domain of high-performance, low-power computer architecture and design. Besides sharing the OPERA project results, attending the HiPEAC events also allowed OPERA to create important connections with other Horizon 2020 projects.