LOw Power Heterogeneous Architecture
for NExt Generation of SmaRt Infrastructure and Platforms
in Industrial and Societal Applications

Meeting minutes 3

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ACRONYMS LIST

Acronym	Description
ADAS	Advanced Driver Assistance Systems
ALM	Adaptive Logic Module
ANN	Approximate Nearest Neighbour
API	Application Programming Interface
BSP	Board Support Package
CAPI	Coherent Accelerator Processor Interface
DCNN	Deep Convolutional Neural Network
CNN	Convolutional Neural Network
CPS	Cyber-Physical System
CPU	Central Processing Unit
DiaB	Datacenter in a Box, a hardware product of the OPERA project
DSP	Digital Signal Processor
ECRAE	Efficient Cloud Allocation Engine
FD-SOI	Fully Depleted Silicon On Insulator
FF	Flip-Flop
FPGA	Field Programmable Gate Array
GPU	Graphics Processing Unit
HiPEAC	European Network on High Performance and Embedded Architecture and Compilation
HPC	High Performance Computing
HPS	Hard Processor System
KB	Knowledge Base
KNN	K- Nearest Neighbour
KVM	Kernel-base Virtual Machine
ISA	Instruction Set Architecture
ISP	Image Signal Processing
LXC	Linux Containers –a specific implementation of the container technology
LXD	Linux Containers – an easier to use interface to manage containers
NIC	Network Interface Card
PCIe	Peripheral Component Interconnect Express
PSO	Particle Swarm Optimization
RAM	Random Access Memory
RDMA	Remote Direct Memory Access

RDS	Remote Desktop Service
RoCE	RDMA over Converged Ethernet
SaaS	Software-as-a-Service
SoC	System-on-Chip
UC	Use Case
ULP	Ultra-Low Power
VDI	Virtual Desktop Infrastructure

EXECUTIVE SUMMARY

This document reports the meetings and the phone calls of the OPERA project for the period M21 (01/08/2017) to M28 (31/03/2018). This document would support the periodic report (D1.3) with the details about the actions and discussions taken during meetings and calls.

Position of the deliverable in the whole project context

This document is the third of four reports for the meeting and calls organized within the project.

The last report will be released at M36, with the final project report (D1.4).

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1 GENERAL ASSEMBLY MEETINGS

1.1 GENERAL ASSEMBLY – NANTES 21-22 NOVEMBER 2017

The OPERA consortium met in Nantes, France, the 21st and 22nd of November 2017. The main topics discussed are organized by WP.

1.1.1 WP1

During the management section the following topics have been discussed:

- Preparation of amendment for WP5 reorganization. The actual description would be enhanced with specific explanations for the modifications proposed.
- Presentation of the outcome of the review with the EU commission and report on the interim payment.
- Report on the status of the deliverables and reminder about the incoming documents.

1.1.2 WP2

The main topic discussed in the definition and implementation plan for the offloading features.

1.1.3 WP3

The installation 1 features and requirements have been analysed, considering the definition of the next prototype. The use of the 3g device connected to the ULP sensor node is needed for debugging, so it will be kept also in the second prototype, and it will be removed only for the final prototype, considering the power consumed by such device, not needed for the functionality of the system.

One open point regarding the first implementation is the finalization of the SPI interface. It is very urgent for the next phase of development.

The discussion on the integration plan for the Orlando platform is started. The target date for the first prototype with Orlando is January 2018.

The first version of cycle detection can be derived from the ST existing implementation of object classification based on AlexNet.

Neavia will study and check for software and platforms suitable for FPGA acceleration.

1.1.4 WP5

The amendment of WP5 need a complete description with motivations. Complete the description of the WP5 Amendment.

Containerization of ULP software to be integrate to LP software for offload analysis.

1.1.5 WP6

The Altera issue for CAPI unavailability is discussed and alternative plans are considered. The partners should identify the platform to be used by Nallatech due to CAPI issue. Nallatech will check for OPAE release.

Discussion on Micmac issue: the open source software is very badly designed and written. For HPE the porting to OpenCL is very difficult.

The issues should be handled carefully, ISMB will take the responsibility to define a plan for the next months. Some issues related to difficulties reported with MicMac, but it seems also that HPE Is not able to work on the porting to FPGA.

ISMB will as ask a detail report from HPE to understand how proceed and action/recovery plan.

1.1.6 WP8

IPR management: the management of IP generated or used in the project is critical for the exploitation and the commercialization. The industrial partners should check internally if they can be selected as IPR manager for the project.

Important remark to TECHNION: the activities on dissemination and publication should be increased. A special attention of the reviewers will be focused on this.

Discussion on gadget/ID cards: The possibility to realize gadgets does not encountered the interest of several partners, the decision should be evaluated considering the budget available that the consortium would allocate. Regarding the customized ID cards for the project is feasible, and the list of interested partners will be created.

1.1.7 WP7 and Demos

1.1.7.1 T7.1- Traffic monitoring use case

The discussion has been oriented to the definition of the potential first use of Orlando in the second system with power grid, without solar panel, with 3g connection.

1.1.7.2 T7.2 - Truck use case

New measurements will be taken on Truck with photoscan and MICMAC.

The MicMac issue should be solved, we don't have relevant results so far, and the deliverable for March is at risk.

1.1.7.3 T7.3 - VDI

The test on 240 concurrent users loads the Moonshot only to the 12%, already improving the power consumption. A test with more users, to push the workload to higher level, can highlight grater improvements. The issue is that for the tests the equipment of 1000 or more users is very complex. Some alternative solutions will be discussed.

CSI takes the responsibility for the stress test definition.

1.1.8 General action points

- ISMB will organize monthly calls for status review with WP leaders
- The issues considered during the F2F will be considered as soon as possible during the WP calls.

1.2 GENERAL ASSEMBLY – AMSTERDAM 5-6 MARCH 2018

The general discussions during the F2F have been focused on the organization of the third and final period of the project. The next F2F has been organized for June, in parallel with the SYSTOR conference in Haifa, Israel. The OPERA project will be presented at the conference for the dissemination activities of the project.

1.2.1 WP2

In this phase the activities in the technical work packages are considered globally in the WP2, as entry point for the consolidation of the results of the second state go development that is ending at the end of March.

An overview of the status of the lesson learnt study is discussed between partners. The results are partially consolidated in the deliverable D2.10. In parallel the document regarding the innovation potential is considered, evaluating the innovation introduced by the second phase of the project. The analysis will be reported in the deliverable D2.7. Both the deliverables are expected for the end of the month.

We need to highlight new parts since the last deliverables, for example for the LL: evolution since the last deliverable, new issues and targeted solutions:

- Highlight that we implemented the CNN on FPGA that is in line for the offloading
- Nallatech provided a new BSP that enable the use of FPGA-SoC (ARM) to be accessed as standard pure FPGA, w/ intel x86_64 host processor as the master.
- NALLATECH is acquiring the DG-station for starting training
- HPE with the MicMac has done some experiments in porting the ANN/SIFT algorithms to FPGA. They created an OpenCL version for the targeted functions although they target a GPU device (not the actual FPGA):
    - The initial results suggest that the functions scale bad on parallel devices: NALL suggested to try to port as much as possible portion of the code within the device to extract more performances (now performance on multicore are better than on GPU -- theoretically possible but to be explained from a technical viewpoint)
- We need to update the architecture of the OPERA+offloading so that the optical connection through a pair of FPGA cards is removed. Now we have ConnectX-5 on the Power8 machine. It uses the RoCE RDMA protocol.
- We need to train both the networks with dedicated classes and images provided by ISERE.
- With NALL and IBM we need to create a container that can run the FPGA Yolo network. Later we can move also for the MicMac.
- The first version of CNN on FPGA provided good results, so we are going for a new optimized version that can use binarized weights for improving performance and still keep the energy efficiency (w.r.t. GPU)

1.2.1.1 MicMac activity

The software makes processing through a workflow: extract tie-points, matching points in images, etc.

All these processes are launched through a set of commands. HPE has profiled the "tapioca" command. This command actually runs the SIFT and ANN, which can be targeted for acceleration. All the commands (workflow) are managed through a 'makefile'. Since the ANN error is set in the MicMac to 0, this can be replaced by KNN. The KNN is easier to be ported on FPGA.

HPE performed some preliminary tests on porting the SIFT algorithm on GPU (Intel embedded GPU), using an OpenCL implementation. The results are not really encouraging.

1.2.1.2 CNN

Richard had to modify a little bit also the activation and the max-pooling layers. For the former, because it is not efficient in performing the non-linear operation. The latter, because it was (my kernel version) too generic. But since we have in Darknet-19 only 2x2 max-pooling filters, Richard restructured the code to be more efficient in performing the operation.

1.2.1.3 Offloading

IBM+NALL can provide the containerisation for the CNN and the access (communication port and daemon for managing the receiving process of images and running the image processing). NEAVIA can provide the integration software for running the bicycle counting.

1.2.1.4 ULP node review

The features and requirements of the Orlando board have been discussed. A plan for the next weeks has been defined. The Orlando board includes natively an interface for the Nucleo board, so part of the software development of the first prototype will be ported on the second one.

A debugging session for the code of the first prototype has been organized during the last part of the F2F.

1.2.2 WP8

A demonstration video for the OPERA results have been created by CSI with the support of the consortium.

- CERTIOS suggested to specify the power consumption not in W but actually W*h

2 TECHNICAL SPECIFIC MEETINGS

2.1 ULP AND OFFLOADING INTEGRATION – GRENOBLE 29-31 JANUARY 2018

Several partners of the consortium organized a meeting in Grenoble from the 29th to the 31st of January 2018. The main purposes of the meeting were

- the consolidation of the computing continuum for the bicycle counting application on ULP and sever sides
- the review of the study of the MicMac framework and the evaluation of the results obtained so far
- the completion of the first prototype enhancements and fixes
- inspection to the second installation site near Grenoble

The partners that attended the meeting were HPE that hosted the meeting, STMicroelectronics, ISMB, Nallatech, Teseo, CERTIOS, CSI, ISERE and Neavia.

2.1.1 Offloading feature

The outcome of the meeting has been a detailed architecture draft of the offloading mechanism applied to the cycle counting use case. The implementation plan has been detailed in terms of hardware setup, communication and software development.

The basic principle is to detect the bicycles and count them on the ULP platform. On this platform a tracking application can evaluate the quality of development. In case of too many bicycles the detection can be less accurate, so a set of images is transmitted to the Moonshot server, that implements the same CNN used on the ULP node, but with an higher quality of detection due to the higher capability of the server, the greater amount of memory available. The acceleration of the FPGA elements in the server will provide a real time responsiveness of the system and will increase the counting accuracy.

2.1.2 MicMac framework analysis

The issues encountered by HPE have been shared between the other partners. A detailed analysis of the code has been conducted. Some element of the framework has been identified as good candidates for the acceleration by FPGA. The support of Nallatech to the HPE activities will speed up this process.

2.1.3 First prototype modifications

The partners involved in the development of the software for the ULP node organized a shared development sessions in order to fix the last issues on the communication. The SecSoC code have been adapted to the Nucleo transmitter code, and the full system has bene tested against different conditions.

2.1.4 Inspection of second installation site

The installation site for the first CNN prototype installation have been inspected by the technical partners in order to identify eventual critical issues. The orientation of the camera has been modified on order to cover a portion of the road from a higher distance and with a greater angle. The installation plan for the receiver is confirmed.

3 PHONE CALLS

3.1 WORK PACKAGES CALLS

3.1.1 WP2

In the period under analysis the main activities of the WP2 have been:

- Synthesis of the results of the project in terms of innovation potential. The outcome of this activities is included in the deliverables D.26 and D2.7.
- Analysis of the progress of the project, in terms of lesson learned, and consolidation of this information in the deliverables D2.9 and D2.10.
- Review of the recommendation of the EU experts.
- Offloading definition and discussion.

3.1.1.1 2017-09-13

Discussions on the finalization of Deliverable D2.6. The deliverable is almost complete, some contributions need to be integrated. Certios provided an update of the current deliverable status. HPE should provide inputs and contribution on technologies that can be part of innovation potential of OPERA (e.g., discussing about the innovation provided by the newly designed chassis, etc.). HPE is preparing a whitepaper (on how to take measurements on the servers, e.g., the Moonshot server) that can be used for both reference and content of the D2.6.

Reviewers highlighted that there is a mismatch between initial claim of server scalability (180 server nodes, but using the original Moonshot server, and the 16 nodes supported by the current chassis -- the EL4000). We need to update both the online tool for collecting requirements and put that also on the next Lesson Learned deliverable.

CSI will update the online tool used for collecting requirements/constraints with the server requirements: scalability to 180 is not achievable with the new chassis (EL4000), but it can host correctly the FPGA cards; also, it is only 1U against the 4.3U of the original Moonshot server.

Certios has a vision on how to take measurements on energy/power efficiency for the whole OPERA platform that we are deploying in the traffic use case through the offloading feature. To this end, Certios will prepare a small document (see WP7, Task T7.1).

Certios and ISMB discussed on the integration of the power/energy measurements and workload characterization, with the orchestration module developed in WP5. Certios suggested to read the following document for such kind of integration: Energy/Power function brainstorm for improving D4.1.

3.1.1.2 2017-09-27

ISMB introduced the main objective of implementing the offloading feature. The idea is to allow remote ULP devices running the image detection software to request some computation (offloading) to a service running on the Isére data center on an EL4000/EL1000 server. The server can be equipped with the FPGA card for acceleration of the computation. The following points have been discussed:

- Switching mechanism: no particular requirements have been indicated (at this phase of design/implementation) regarding the way the ULP can contact the remote server
- Remote server: the actual chassis that will be used for experimentation is the EL1000, since the application requires only one cartridge and it has more storage space on board. In addition, it can still host the Nallatech FPGA board
- The software used for the detection on the ULP side, is based on some feature exposed by the new Orlando platform. Specifically, the ones that allow to accelerate the CNN (Convolutional Neural Network)

    - STM used a CNN model described using the Caffe framework;
    - Nallatech has some experience in accelerating the Caffe models on the FPGA (this solution is better than emulating on the FPGA Orlando features): http://www.nallatech.com/fpga-acceleration-convolutional-neural-networks/
    - For accessing the FPGA board from a container, the simpler solution (already tested by HPE in other context such as HPC): both the host system and the container can install the same driver, so there is a link one to one between the driver on the host and the one running on the container;
    - The software for the detection on the ULP and the one running on the EL1000 system are not the same;
- The software used to counting bicycles on the server side, is based on the Caffe model used by STM to generate the version optimized for the Orlando ULP. Such soft model is wrapped by a container;
- The server side needs to have two containers: one managing front-end operations (waiting the ULP sending an image to analyse, and eventually to send back some result). This container is responsible to turn on the worker container which is running the Caffe CNN model;
- The use of (embedded) GPUs to accelerate the CNN soft model should be avoided for two reasons:
    - To larger power consumption, especially when not embedded on the CPU processor;
    - The reviewers (as highlighted by CERTIOS) are interested in seeing all the technologies developed and integrated in OPERA working on the same use case;

The next audio meeting will target more specific implementation issues, in order to refine the proposed solution.

3.1.1.3 2017-10-11

The requirements and implementation of the offloading feature have been discussed. To this end, the attendees discussed basically how to import the CNN model exploited by the ULP to the FPGA card and the software requirements to run the ULP cycle counting application on the remote server.

- Nallatech already have implemented a CNN model (supporting the Caffe API) on a Stratix-V device, and it is working to port it on a Stratix-10 and Arria-10 devices:
    - Porting requires minimal adaptation and recompilation to exploits the highest parallelism of the Stratix-10 and Arria-10 devices. On the other hand, the code can be only recompiled (synthesizing again the circuit for the new target devices, but losing the performance gain);
    - It will be necessary to see what kind of support the NEAVIA software requires for running the CNN. This implies to understand how the software exploits the ULP acceleration features, and try to replicate them on the FPGA device;
- We need to understand clearly how the container application can access the FPGA board on the server side:
    - Gallig Renaud (HPE/Nallatech) said that it is possible to create a link by installing the board driver twice:
        - One time on the host;
        - A second time on the container;
- The application is not intended to be as multi-user, only a single device will send the information to the server. Thus, the FPGA is not shared across multiple software instances, but only by a single one running the NEAVIA software.

3.1.1.4 2017-12-06

The audio meeting has been devoted to discuss current progress for the offloading mechanism, as well as specific issues/open points on the architectural design.

Software application for bicycle counting

The software used to perform traffic monitoring in the context of bicycle counting use case is the same both on the ULP device and the remote server. The application is composed by a software block that performs analysis of the images captured by the ULP camera, and a block accelerated directly by the ULP. This latter block runs a CNN which architecture is based on the Tiny-YOLO network. The load estimator should be implemented by STM using functionalities of the ULP device. However, YOLO and Tiny-YOLO provide capabilities for performing multiple object detection and also object tracking (sequence of frames). The NEAVIA software uses the output of the CNN to perform further analysis on the images and counting bicycles.

Server side

The server machine (X86_64 node) that will be devoted to perform bicycle counting analysis should be located in Dept. ISERE headquarter. It is based on a Moonshot chassis provided by HPE. NALL will provide the FPGA card and necessary help for installing the acceleration card and the software (runtime and BSP for the OpenCL). NEAVIA does not see any specific issue to port the software on the X86_64 node. Since it uses the output of the CNN, interfacing the software with the (accelerated) YOLO network should be transparent. YOLO-version 2 (i.e., Darknet-19) should be ported easily on the FPGA device (from a first estimation by NALL, the whole set of CNN layers saturate the Arria-10 device, so no room for accelerating further functionalities). CERTIOS suggests to perform comparison running the software for bicycle counting in three different contexts:

- The software and CNN run entirely on the host system (X86_64 node)
- The software and CNN run entirely on a Linux container on top of the host (X86_64 node)
- The software on a Linux container on top of the host (X86_64 node), while the CNN is accelerated in hardware on the FPGA Arria-10 based card.

3.1.1.5 2017-12-15

Reviewed the progress of FPGA setup at ISMB.

Waiting for new BSP to be released this week.

Compiled examples from Intel.

Reviewed FPGA architecture proposed by Nallatech.

The actions proposed during the call have been:

- ISMB getting up to speed on OpenCL architecture.
- ISMB to look at implementing simple activation layer kernel and integrate into Darknet-19 stack.
- NALLATECH to the same with the convolution layer.

3.1.1.6 2017-12-20

The audio call was restricted to HPE, Nallatech and ISMB partners to discuss on offloading mechanism implementation. During the audio call the following topics have been touched:

- Acceleration of the YOLO network: the initial target is to integrate small kernel into the YOLO-network code. Nallatech and ISMB agree to consider as a starting point the implementation of the leaky activation function (this is the default activation used in the YOLO network). ISMB started to track the chain of function calls to determine the exact point of insertion of the kernel code. After this step, the integration of the convolutional layer acceleration should be easier. Nallatech will provide support for the optimization of such accelerated functions.
- Acceleration of MicMac code: at the moment the main difficult is represented by the way the original code use multi-threading. It is difficult to limit the number of parallel thread running and using the acceleration function. This could be solved by using future OPAE extension from Intel.

Up to now, HPE is focusing on some functions and algorithms used by the orthophoto software such as ANN (i.e., approximate nearest neighbor).

3.1.1.7 2018-01-17

Updates on the progresses in porting CNN and ANN algorithms to FPGA.

ISMB and NALL are almost ready in terms of material to present in the results at the HiPEAC conference 2018 in Manchester.

NALL is planning to have a technical talk at the 6th International Workshop on OpenCL (Oxford, UK, May 14-16, 2018) on the acceleration with FPGA of CNNs.

- A binarized version of the YOLO9000 is presented in a paper (see Darknet official website: https://pjreddie.com/publications/) and is potentially very interesting as a FPGA target:
  - ISMB shared the paper with people attending the call.

Convolutional Neural Network based on YOLO9000:

- Convolutional layer written by Nallatech:
  - Convolutional filtering.
  - Coefficient loading.
  - Temporary result caching.
- Activation layer written by ISMB.
- The current code is loaded, shared and managed using a Github repository.
- Estimated performance of the convolutional network are very good, and when moving to performance/Watt still better than using a conventional GP-GPU.
- Nallatech shared some results on the FPGA resource usage and regarding the convolutional layer implementation: it uses several MADD operation in parallel, to achieve several GFLOPS within a near 20W power envelope.

Nallatech is planning to create a new BSP for the board 385O (the one equipped with the SoC ARM), in such way the board can boot up without setting by default the ARM sub-system as the master. In this way, the board can be accessed and used by the host server processor in an easier way.

Nallatech is planning to buy a workstation with multi GP-GPU cards:

- Need >= 3 GP-GPUs (possibly Quadro from NVIDIA or AMD FirePro):
  - Actual no good choices from Dell and HPE
  - Possible solution to buy a DGX-station (~50k)
- Nallatech suggested to express the will of buying such workstation to:
  - Better tuning YOLO9000 network and tiny/pico YOLO (i.e., better specializing the training for bicycle counting).
  - Eventually comparing in terms of performance/Watt the implementation with FPGA.
  - Decision on which actual hardware to buy will be taken during the next HiPEAC event in Manchester, and finalized during the next F2F in Grenoble.

HPE is working on several potential algorithms used in MicMac to accelerate with FPGA:

- A report is on going
- The main focus is on ANN (a version of the Nearest Neighbour algorithm) for the FPGA implementation.
- Also other algorithms are under investigation.

3.1.1.8 2018-02-14

The audio call has been focused on the planning for the preparation of the deliverables for lesson learned and innovation potential.

3.1.2 WP3

3.1.2.1 2017-09-13

The call has been devoted to:

- The review of the new version of the deliverable D3.1, and the missing parts to be added for the resubmission.
- The setup of a private area for data and code sharing, hosted by STMicroelectronics and shared among the WP3 partners for the joined development of the code for the ULP node. The platform is named STForge.
- Started the discussion on the usage of Orlando platform
- Report on the issues for the communication between SecSoC and Nucleo through the SPI interface
- Report on the progresses for the 360° antenna

3.1.2.2 2017-10-03

The setup of the STForge access on going, the security rules implemented for the access to the system need a detailed configuration.

Hardware setup and integration

New board from TESEO available within few days for the integration of SecSoC and Nucleo

A new optical zoom with 4x fixed will be available. NEAVIA should check if it is fine for their algorithm on the first test site.

Software development

The release of the wrong way detection is expected for the end of October.

Action Points

- The Table of Content of deliverables D3.6 and D3.3 to be released within 2 weeks (TESEO and NEAVIA)
- Report on the new integration board when available (TESEO)
- Organize a physical meeting between STM, ISMB and TESEO for the integration and the first power consumption tests (STM)

3.1.2.3 2017-10-17

Problems related to SPI communication

It is agreed that the involved partners commit in the code versioning platform made available by ST the following:

- Code running on the SecSoC (NEAVIA)
- Code running on the Nucleo board (ISMB)

TESEO should send the new board to ST for validation. Once this is done (or in parallel) physical and/or remote meetings could take place among the involved partners to solve open problems if necessary. Since the antenna is in the ISMB premises, the test of the complete system should be done in ISMB premises.

Software status and Use of Orlando

NEAVIA is currently working at the wrong way detection application (second Use Case scenario).

The third Use Case scenario (cycle detection) should involve the use of the Orlando ST platform. Boards of this platforms should be available during the second half of November, too late for the time frame of March 2018 when the third scenario should be available. It should be possible to delay this deadline if Orlando is used. Anyway it appears that the use of Orlando in the third scenario is not a choice. If available

(ST will check internally) a board will be sent to NEAVIA as soon as possible (before November). In parallel, NEAVIA will perform an evaluation to understand which type of Neural Network they need for the detection and with what effort this can be mapped to Orlando. ST will provide examples of how to map a Neural Network to Orlando.

3.1.2.4 2017-10-24

The code versioning tool made available by ST is running and currently used by the different partners. NEAVIA could upload the latest version of the software.

The new boards of Orlando will be available during the second half of November, no boards of the previous set are currently available.

NEAVIA asks to use in the communication between SecSoC and Nucleo board the same protocol as the one they use for communicating between the SecSoC and the MiniPC embedded at the base of the pole (Use Case scenario 1). NEAVIA agrees on describing this protocol in a document.

Input is needed for deliverable D3.6 (by TESEO, deadline end of November, should be available for internal review by mid November).

Also deliverable D3.3 should be completed during these weeks (by NEAVIA, same timeline as D3.6).

3.1.2.5 2017-11-07

D3.6 received most of the contributions, and they all seem to be ok.

D3.3: some contributions are still missing, NEAVIA should send an email to all partners whose contribution is missing

Board/interfaces SecSoC -> Nucleo: a board will be sent to ST within this week for replicating the problems TESEO is encountering

All WP3 task leaders should send to ST some slides with an update of their activities (F2F meeting in Nantes)

3.1.2.6 2017-12-05

ISMB provided the code using the SPI to ST.

There has been a discussion about the problem related to the heights of the receiving and transmitting parts which are apparently different for the second site, problem related to the fact that the new steering antenna cannot be inclined, but finally it has been stated that this is not a problem, because the relative position of the receiving part and of the transmitting part will be fixed and will not change.

The visit of the second site is scheduled for next week.

Some Orlando boards have been delivered to ST, one or two of them will be sent to NEAVIA as soon as possible. The decision is to map a Tiny Yolo neural network on the Orlando and a fully-fledged Yolo on the FPGA server for remote detection. It has been proposed to NEAVIA to start training the Tiny Yolo as soon as possible, since this training can be done on a PC and does not need the Orlando boards.

3.1.2.7 2017-12-19

SPI problems still exist and need to be solved as soon as possible. On January ST and ISMB should work together trying to solve this issue.

The decision on the second site has been restricted to two possible sites, one of them is more complex from the detection point of view because the scene can contain both bicycles and cars. The Neural Network that was chosen to be implemented on the Orlando platform (Tiny Yolo) should be able to detect bicycles even in complex scenarios like this. Anyway, the decision on which of the two candidate sites to

choose has been postponed to beginning of January, once the capabilities of the Tiny Yolo will be evaluated.

The Tiny Yolo is going to be ported to Orlando by ST. ST will report to the other partners if the Tiny Yolo was modified before port to Orlando.

3.1.2.8 2018-01-16

ORLANDO board sent to NEAVIA.

Communication among SecSoC - Nucleo board - Transmitting Antenna - Receiving Antenna - Nucleo board - Raspberry needs to be finalized and tested.

It's necessary to start as soon as possible activities for installation of cycle detection use case: activities should be parallelized as much as possible. E.g. box realization should be parallelized with software development.

3.1.2.9 2018-02-06

Step 1 and Step 2 of Communication between SecSoC and Remote Server could be done in parallel, after the current version of the communication software is committed to the GIT repository.

The time needed to wake up Nucleo, WiFi module and antenna and establish a connection with the receiving part (always active) is of about 5 seconds. This time should be taken into consideration in order to evaluate the impact of a complete power off of the transmitting part when it is not needed.

ISMB started to study how to turn off and turn on the communication modules on the transmitting part. Roberto should collect this information and investigate on the impact on the existing hardware.

Use Case 1 (traffic congestion + wrong way detection) sends one frame every minute (for debug purposes / this interval can be extended) and then one frame for every event. If events do not occur very frequently (e.g. less than one event every 15 or 20 seconds) a single buffer (other than the buffer used by the JPEG encoder for encoding each frame) should be sufficient for storing the frame that needs to be sent. This buffer can become available again once the transmission of the frame is complete.

3.1.2.10 2018-02-13

Modification of the packet (adding a trailer) by NEAVIA should be done within this week.

ISMB experienced problems in committing his code on the GIT repository, he should retry today. In case of problems, he will contact ST for support.

ISMB is waiting for information on the format of the packet trailer by NEAVIA.

Regarding the CNN training, a first training will be performed by ST on a subset of the COCO dataset with the following 6 classes: bicycles, motorbikes, cars, buses, trucks and people.

3.1.2.11 2018-02-27

NEAVIA completed the modifications needed in the SecSoC for communicating to the Nucleo board. The software on the Nucleo board is not updated and completed yet.

There is need for a physical intervention on test site 1 for updating the software on the Nucleo boards (transmitter side and receiver side), it has been asked to ISMB to be ready for this Thursday or Friday (March 1st or 2nd), in order to complete everything and have time to write results about this in deliverable D7.2.

Regarding bicycle detection, ST is starting the training of the Pico YOLO.

3.1.2.12 2018-03-13

The first full communication test on the site didn't achieved the expected results. ISMB will do some more tests in lab for fixing the different parameters especially on the receiving side and go again to installation site 1 to test the communication.

The communication between the SecSoC and the Nucleo uses a CRC code to verify the correctness of the transmission. Some problems of the value of CRC have been detected, and should be fixed as soon as possible. ISMB will update the SecSoC SW and redo all the tests on the Nucleo board to see if all problems are fixed. When going to installation site 1, ISMB will also upload the latest version of the software on the Nucleo board.

Poor JPEG quality obtained in the latest version of the SecSoC software could be an electrical or timing problem of the sensor or the JPEG encoder, ST suggested to reset the system to see if the problem is solved. Otherwise, it could be related to the JPEG size, which could be too small (high compression ratio).

Wrong way detection application development is ongoing.

Problems that still need to be fixed in 1st installation site:

- Communication SW
- Issue related to communication distance (hopefully both will be solved between this week and the beginning of next week)
- Board for turning off Nucleo board, Wi-Fi module and antenna when not needed --> ST has to inform TESEO about what GPIO to use in the SecSoC for performing this operation

3.1.2.13 2018-03-27

A physical intervention has been organized for Thursday March 29th in test site 1 to test communication.

3.1.3 WP4

3.1.3.1 2017-08-23

The call has been devoted to the analysis of the recommendations provided by the reviewers.

D4.1 rejected again - how to make it work?

- It is not a rejection but a revision. ST will send around the review documents.
- We need to elaborate more on the reasons why we have made some choices.
- 5.2 section, elaborate in why the memory mapping.
- The revised version of D4.1 needs to be delivered before Sep 30st. CERTIOS asks ST and ISMB to get into contact with the reviewers as the comments are high level and there is a strong need for more clarification as issues are raised that were not raised during the review meeting of M18.
- CERTIOS will write the points in a more extensive ways to guide TECHNION for improvement of the section 5.2 in D4.1.

3.1.3.2 2017-09-06

D4.1 revision progress

The purpose of this call was to discuss the subject of the reviewers' comments on the second version of D4.1.

To facilitate this discussion, a brainstorm document has been created on google docs, under WP4 work in progress.

- Primary input into the discussion came from the dialog between Joel and Dirk in discussing

a. What would be the output of a function that is needed to steer the workload placement and node control of a heterogeneous cluster.
b. Which parameters form the input and how to define an efficiency model.

As to a., efficiency hinges on the concept of work (or even useful work) but given that the object of the datacenter is to provide services 24X7, Power needed to deliver on the SLA that describes this work seems to be a good starting point.

As to b., the work described in the remote desktop use case will be fulfilled by breaking up the applications into micro services. These micro services have their own request queues. For efficiency these queues should not be too short, for fulfilling the SLA, these queues should not be too long, request should be handled within a described time limit.

It is feasible that this queue length could be a manageable parameter that would be usable in steering/optimizing efficiency.

On a separate note, given a number of possible nodes that are usable to fulfill the SLA, having a graph that describes the power-draw of each node under certain measurable conditions and combining that with (observed) behavior of a workload can be used to minimize the power draw while fulfilling the SLA.

The explicit question was raised whether describing a model in such a way had an inhibiting influence on the work in other OPERA tasks. There was no response that indicated that such an influence existed.

Actions

IBM posted a link to the paper "slower is faster" as an inspirational paper".

IBM will formulate his thoughts on the model definition.

Everyone will read D4.1 with the reviewers comments in mind and additional thoughts and comments will be placed in the brainstorm document on google drive.

A meeting will be held coming 11-9-2017 to be planned and chaired by CERTIOS.

3.1.3.3 2017-09-11, 2017-09-20

The September calls have been focused mainly on D4.1 revision progress.

CERTIOS explains about D4.1 extra Chapter.

Dirk asks HPE, Nallatech and TECHNION to read this new Chapter carefully, as it has consequences for the other WP's.

3.1.3.4 2017-10-04

D4.1 has been delivered with an extra chapter, aimed to solve the reviewer's remarks. This chapter may have consequences for other Tasks under WP4, especially for the work of Nallatech. That is the reason that an extra online call between CERTIOS and Nallatech has been set up, for exactly one week after this meeting.

Discussion consequences D4.1 for the other WP's and D4.X's.

- Because of the possible consequences of D4.1 for each of our tasks, CERTIOS asked people in the meeting to make sure that everyone has read the Chapter 6, and is aware of its content and will ponder whether this may have consequences for the OPERA work at hand.

3.1.3.5 2017-10-11

Discussion and planning about the impact of the WP4 modification, described in D4.1 for the other WP's and for the next deliverables of WP4.

3.1.3.6 2017-10-18

Preparation and consolidation of the quarterly report of WP4 activities.

3.1.3.7 2017-11-01

Dirk gives an 'early warning' that before the F2F in Nantes, he may need input from the different WP4 partners. Cross over interests and activities will be discussed there. When the meeting will be further organized, skeletons for presentations are expected and to be filled.

Next deliverables

D4.7 will be finished on time by IBM.

Progress

On schedule.

Task 4.3

Nallatech is working on monitoring software, as an add-on for RedFish to retrieve information from the CPU (MSR register). Intel is delivering specific registers for monitoring. These will be used to record the DDR power use. Question: is there a same capability on the IBM system? The answer is yes, IBM has these kind of solutions probably 3 years before Intel does.

PERF-L standard tool in Linux is suitable for that kind of monitoring. All of this kind of measurements is accessible via this tool. There are some other ways (Happy), there are different counters too, and there is a wealth of possibilities, so we really have to make choices.

If possible we will work with the same tool (for IBM and HPE).

3.1.3.8 2017-11-29

Task 4.3 Status update

Alberto reported on the progresses on workload management.

HPE will create a report on the power analysis of the MicMac profiling.

Acceleration of FPGA is now ongoing.

TECHNION is currently working on profiling applications.

Applications run faster in a virtual machine then on bare metal. Different kernel parameters cause this.

CSI should supply these applications. It will be discussed in next call.

3.1.3.9 2017-12-11

Task 4.2 progress

Task 4.2 is progressing well. Current tests are still manual, automating VM creation and measurements.

TECHNION Idan will contact CSI on the collection of applications that are used in the VDI casus.

Task 4.3 progress in measuring the effect of efficiency measures

Profiling is done, in terms of CPU usage not yet in “power” will be done during the training in Grenoble.

Current status is that an FPGA resource cannot be shared between multiple treads.

CSI still needs to run the Photoscan PRO without GPU acceleration (CSI is in contact with Nallatech on this).

CSI updates on the load generator: current licenses are for up to 900 virtual users the first assumption is that this will create a CPU load of around 50%.

- Possibly need additional licenses
- Possible other solutions in choosing a different cartridge
- First order of business is to test with the currently available licenses.

Traffic Monitoring use case has no updates at this point in time. The second test case is currently being evaluated.

3.1.3.102017-12-18

PhotoscanPRO execution without GPU is scheduled for beginning of January 2018.

Licenses for load generators are very expensive, other options are being explored

- Options include an open source load generator

FPGA monitoring is being further developed, FPGA info needs to be passed through the BMC (discussions with HP ongoing).

Development of the measurement tool leveraging “perf” by Nallatech is ongoing

- FPGA will be monitored with Redfish
- Moonshot and power8 will be monitored using the “perf tool”.

Nallatech will share the monitoring scripts with IBM that will identify and correct any gaps on the power8 machines.

TMC camera: the second test site is still being discussed (see WP7 call). Issue with this second site is that the distance between sender (reconfigurable antenna) and receiver (reconfigurable antenna) is very small in the second site.

Preliminary measurements showed a surprising result that the energy used when sending a packet is independent of the distance between sender and receiver. This is still being investigated as this result is not expected. At this point in time it is most important to get the entire system working (independent of distance) later in 2018, separate test to determine maximum separation between sender and receiver including associated energy use will be scheduled.

Task 4.4

Due to reasons explained in WP5, creating the optical link between Moonshot and power 8 using the OPERA developed FPGA board is no longer feasible. Instead a commercially available board will be used.

Current option is Rocky RDMA from Mellanox. IBM acquired this card but in order to get it working over Ethernet it needs a firmware update. Mellanox promised to deliver this update since the documentation indicated that this was a supported option.

3.1.3.11 2018-01-08

Task 4.2 progress in memory management, progress in application profiling

Checks, and all kinds of preparations for 2 TECH activities:

- benchmarks
- simulations (some results were expected to be higher).

TECHNION followed suggestion to contact CSI, that said that they can't share workloads, so we need to stick to the Spec benchmarks. CSI was also going to look at open source not discussed with Idan. Hopefully to provide them in a few months, so we can integrate with the framework of TECHNION.

Task 4.4 progress in interconnect development and energy measurements

IBM: The lines are a bit blurred right now between WP6 and WP4. It got a new firmware build from Mellanox that supports the ODP feature for RoCE, and have been working hard to test it. It wrote a program that can copy a memory page (over RoCE on-demand) in userspace, but haven't yet measured its latency. It is now working on an all-kernel version that should be considerably faster.

Also, it ordered a PCIe interposer that can be used to build a power measurement device for a PCIe card. It is expected to arrive any day now, and then some soldering will be needed.

Task 4.3 progress in measuring the effect of efficiency measures

Still going on, too much to mention in the call. Document is in progress. End of March deliverable. HPE: by the end of Jan all activities will done (MicMac porting). Profiling is finished (still profiling whilst running the energy measuring).

Use case traffic management

No specific news. WP meeting, results of software test at NEAVIA, tomorrow. We will use the sender-receiver is a short distance. Define energy metrics system, there is no issue to implement.

Actions points

Nallatech needs a TOC to startup the deliverable, due the end of March. Nallatech will make a TOC start and will send it around for improvement. NB.: It's an 'early' deliverable compared to the other deliverables in the project. Could the deliverable be postponed? We will discuss this next time.

3.1.3.12 2018-02-05

Task 4.2 progress in memory management, progress in application profiling

Task 4.2 progress is going well. Most of the results are in but are being analysed.

Currently the 2006 benchmarks have been run. The 2017 runs still have to be done.

Preliminary schedule: larger benchmarks will be run in March.

Task 4.3 progress in measuring the effect of efficiency measures

Truck use case

HPE is putting together the MicMac profiling report, expected for mid-February.

Actual acceleration is still far away, but a candidate function has been identified for offloading to the FPGA.

CSI: Photoscan pro and MicMac have been run on the same platform, both non-accelerated this work is very close to being finished.

Use case VDI

CSI has selected a load generation product that is able to drastically increase the number of (virtual) users for testing. First results are expected this month (February).

Containerization is being worked on by IBM and is also close to resolution.

Traffic monitoring use case

Installation on test site has been moved to end of February

ISERE is currently working on finding a system that accurately measures low energy and is able to store these measurements on the test site. The system will need to be able to work in "external" conditions.

3.1.3.13 2018-02-19

Task 4.2 progress in memory management, progress in application profiling

2017 benchmarks are running into issues linked to CPU isolation features (this is a known kernel bug), options are to either forgo running the 2017 benchmark or to skip CPU isolation. Skipping the CPU isolation will, however, provide very "noisy" benchmark results.

There are sufficient good results from the single threaded 2006 benchmark to finish the task but additional results from the 2017 benchmark would have been appreciated.

Task 4.3 progress in measuring the effect of efficiency measures

Use case Truck

HPE released the first draft of the MicMac profiling report.

CSI: Photoscan pro and MicMac have been run on the same platform, both non-accelerated this work is very close to being finished.

Use case VDI

CSI: we have selected a load generation product that is able to drastically increase the number of (virtual) users for testing. First results are expected this month (February).

There are issues with the methodology, results are dependent on the containerization but are expected before the F2F meeting March 5th.

Containerisation of own cloud is finished, this was delivered by IBM to CSI, Open Xchange is currently being worked on.

3.1.3.14 2018-03-19

This call has been devoted to the review of the outcome of the Amsterdam F2F and the verification of the actions for the next period.

Task 4.2 progress in memory management, progress in application profiling

Progress goes well. TECHNION is communicating measurements of 4.2 to NALLATECH. TECHNION is looking for benchmarks for MicMac to integrate in its framework.

Task 4.3 progress in measuring the effect of efficiency measures

NALLATECH is in charge to collect input. The current status indicated by Nallatech is that it has been fully covered. Completed the work on the FPGA, measured power usage during its performance, 1) running MicMac and doing 2) offloading, with the help of Redfish.

3.1.4 WP5

3.1.4.1 21-08-2017

Discussion on the reorganization of WP5

Discussion about the modelling of energy efficiency in the OPERA cluster.

The Redfish implementation can supply us with a list of available fields in both the IBM machines as well as the HP/Intel machine and due to the Nallatech work, also on the FPGA board.

These available fields can possibly be matched to the workload to Energy prediction model as created by Technion.

From this work a formula can then be created that would enable energy usage of the OPERA cluster to be calculated given a certain workload placement.

The formula described above can be analysed and an optimal (minimum energy) point can be established.

WP 4.3 can then be used to obtain measurements that confirm the work described above by actually taking measurements on different workload placements.

This work will be discussed further in the scope of the WP5 task 5.5 and WP4 task 4.1 and 4.3 calls.

3.1.4.2 04-09-2017

IBM on RDMA

- We have implemented SMC sockets
- Not able to beat TCP/IP over Ethernet yet (latency)

CERTIOS

- Not much detail exposed through IBM RedFish implementation
- Probably worthwhile to find another method to show power consumption
- Create a 3D graph (one for each machine type) showing CPU usage & memory usage vs energy consumption
- Option: Propose extensions to Redfish (missing items) which are required for measuring energy consumption
- Option: Write a strategy for how to deal with variability in the measurements

3.1.4.3 18-09-2017

IBM reports some progress on RDMA and compilers.

ISMB

During review it was identified that WP5 deliverables could be merged

IBM suggests to define two deliverables for WP5 (T5.1 - T5.4): one about the orchestration part and one about the infrastructure part.

ISMB

Soon we'll start to integrate measurements into the orchestration system.

Start with existing orchestration system, collect measurements and start transition to the new orchestration system.

Review criticized absence of integration of WP3 with other tasks. We are considering how to integrate complex calculations (e.g bike counting) into server workloads.

WP3 workloads will be implemented in C/C++ and adopted to the server environment

HiPEAC CSW-Autumn: partners are asking to confirm their participation. The session will take place on Oct, 25.

3.1.4.4 16-10-2017

Nalltech

- We need to start organizing D4.3 (measuring baseline for power consumption)

ISMB

- As part of D5.4, wants to run a simulation on Python of the orchestrator - outcome will be 'average power consumption'. After discussions with CERTIOS, he suggested to not measure peak consumption, but average per node over time.
    - ISMB has implemented the orchestrator policy, and aims to have application queues implemented in about 1 month

- It intends to release simulator code as open source - need to find a place (github?) and permissions from ISMB

3.1.4.5 16-11-2017

All the partners have filled in the amendment draft for WP5 reorganization.

ISMB to discuss internally about the merge of T5.3 and T5.4. The division is not clear.

TECHNION to update Section 2.4 description to match with agreement by ISMB on what to provide in terms of monitoring capabilities.

IBM to consolidate objectives for DoA and F2F slides.

WP5 amendment to be presented during WP5 slot at F2F.

3.1.4.6 16-11-2017

Integration between ISMB scheduling algorithm with Technion measurement

- Technion provides math models
- ISMB will implement those models

CERTIOS: we should measure difference between running things on Power, ARM and Intel. We can use simulation.

3.1.4.7 14-12-2017

ISMB: creating a simulator for allocating containers

- Use a mathematical model - has selected a model by <author A> and <author B> published in <paper C> - with emphasis on power consumption
- Started coding simulator, but still looking at some existing simulation infrastructure
- There are simple techniques to use to model queues, so the implementation is not a large effort
- First plans to finish implementation of allocation strategy - hopes to have results by end of Jan, maybe Feb.

Certios:

- Needs input for WP4 from ISMB related to the queue modeling (result from WP5)

Technion:

- Working on Glibc addon
- Trying to control memory allocations flexibly, but using various page sizes automatically
- Started by intercepting malloc() and free() - not a good method, so now moved down a level to intercept sbrk() and mmap() system calls
- Three approaches - glibc, ptrace, dlmalloc - simultaneously to find the most successful results
- Targeting April submission deadline (conference in Aug/Sept)

IBM:

- Using LXD containers - best integration with CRIU
- Containerizing VDI apps
- Still looking at the best options for container migration
- Talked to CSI about deploying containerized apps on CSI testbed

3.1.4.8 11-01-2018

How can we view the input queues of “real life” application components, such as MySQL, Redis, Apache, etc.?

Cloud Lightning (another EU project) has a way of looking at the input queue of a microservice - maybe we can take advantage of their method

ISMB: still coding the simulator

- Aims to have a short paper for Systor (end of Feb)
- Looking at CloudLightining EU project and their simulation infrastructure:
  - https://cloudlightning.eu/blog/cloudlightning-simulator-launched/
  - (WP7) https://cloudlightning.eu/work-packages/public-deliverables/
  - Also looking at published papers:
    - "A framework for simulating large scale cloud infrastructures"
    - "Towards a scalable and adaptable resource allocation framework in cloud environments"

TECHNION

- Still working on the 3 projects mentioned earlier: Libc, ptrace, dlmalloc
- Needs to have some results before sharing algorithm with ISMB

IBM:

- Adding features to CRIU
- Currently working on remote page faults over RDMA (WP6 stuff)
- In about 3 weeks, will get back to workload decomposition (containerization of application components)
- Then the plan is to integrate CRIU post-copy migration with remote page faults over RDMA (in kernel module)

CSI:

- D7.7 - need measurements by end of March
- Need to review the deliverable requirements for Phase II

3.1.4.9 01-02-2018

IBM - finalized amendment with Coordinator (@ HiPEAC)

Needs to test the PCIe riser for compatibility with NIC

Continuing work on CRIU

Starting containerization next week ** PRIORITY to tell CSI by end of the week if we will make it in time for the deliverable @ end of March (including time for testing)

Should target OwnCloud first

ISMB - working on simulation

Needs collaboration with Certios & Nallatech

IBM - need to send info (hotels, travel, invitation letter, Systor registration) regarding F2F in June

Technion - slow progress due to end of the semester

- Working on dlmalloc() allocator (est. 3-4 weeks)
- Plans to submit a paper April/May timeframe

CSI working on deliverable

ISMB

- It has received some solicitation from new potential projects to reuse some of our results

- It will provide more details about potential projects as the details become available

3.1.4.10 08-02-2018

IBM has deployed OwnCloud with containerized services (microservices) at the CSI testbed

Needs OpenStack integration (help from ISMB + CSI)

ISMB + CSI have a call tomorrow to discuss strategy

ISMB has made more progress on the simulation

3.1.4.11 22-02-2018

ISMB demo of the simulation

3.1.4.12 22-03-2018

ISMB is looking at CloudSim - to be used in addition to the Python simulation

The module used with the Python simulation can be reused in OpenStack

Deliverables have precedence - workload consolidation will resume in a few weeks

ISMB working with CSI to integrate TOSCA template to work with OwnCloud

HEAT translator seems to be working - should be ok

IBM is containerizing OpenXChange now

IBM is also integrating RDMA transport for page faults into CRIU - coding hasn't started yet

3.1.5 WP6

3.1.5.1 2017-08-10

IBM CAPI firmware resource issue update

Original development team has been reallocated. The simulation and initial design is complete and new engineer is to be resourced to debug the CAPI interference. The original development team will be available for small amounts of support if required.

MICMAC power profile baseline update

To be done this week. Script completed to talk to the Rest API EL4000. Top 20 processes and their consumption. Script failing after a few minutes (Currently 5 seconds between calls). Creating a bigger delay may help, bug report has been submitted to Rest API team.

MICMAC application profiling update

Tapioca function has been profiled.

Actions

1) IBM provide update the CAPI development team.

2) HPE to profile power still to be done.

3) NALL to install the FPGA runtime tools on HPE server and verify hardware.

4) NALL to review profiling of Tapioca function and project acceleration suggestions.

3.1.5.2 2017-09-07

Power measurements provided through Redfish are currently unlikely to provide sufficient detail for improved performance metrics required in response to modifications made in D4.1. Therefore, it is

proposed that the consortium will investigate what is generally possible through other IP and software to create a baseline. The results of this work will be used to provide suggest improvements to the Redfish interface, with these recommendations fed back to the server vendors (IBM, HPE, etc.).

Actions

1) HPE to investigate what power performance counters are available to the user outside of RedFish.

2) NALLA to complete previous actions 3&4

3.1.5.3 2017-10-04

NALLATECH plans to install and setup SOC firmware in Grenoble

3.1.5.4 2017-10-31

HPE Reporting for the June to September is done.

- Expenses (effort, hardware and travels) are reported

- MM effort is being detailed in the effort file

The data have been shared with the coordinator.

OpenCL Training

HPE won't be coming to the November session (OpenCL basics) as he followed a full week training earlier this year (Acceleware).

Only ISMB and Nallatech for the initial session.

ISMB and HPE will be following the second session that will take place late January in Bristol (to be confirmed).

The goal of this session will be to review the OpenCL code created for both traffic monitoring (ML inference) and Truck (Micmac).

Micmac effort

Power measurement tool to be updated by NALLATECH (current version on Opera server located in Grenoble) goal is to have a monitoring of:

- CPU usage
- Top 10+ functions
- Power usage for CPU, Memory and overall system

HPE to prepare the profiling report for 1st meeting

Preparation to F2F Nantes

Cristian will be representing HPE in Saint Herblain.

Need to prepare 4 to 6 slides for presenting HPE effort on the Micmac porting

- Identification of bottleneck / power profiling

- Potential software optimization

- Selected function to be offloaded

3.1.5.5 2017-11-07

Redfish update meeting

1) Discuss next steps for Redfish API integration.

Schema designed and approved by Mike Garrett.

Two options:

1. To get schema published into the BMC (Board management controller, HiLO, web interface etc). This would require work with HP.
2. Potential write into the BMC memory. Driver in Linux writing into the BMC memory, to publish data from FPGA.

Actions

1. Derek Cameron (Nallatech) to find out how to retrieve data from the FPGA in combination with OpenCL FPGA driver.
2. HPE driver interface is open but not published. NALL will need driver with these interfaces. Gallig (Nallatech) to talk to HPE about getting access to unpublished but open driver interfaces. This will allow the data populated by the NALL driver to be visible to the HPE HiLO diver.
3. Gallig (Nallatech) to produce high level diagram of driver interfaces for clarification.

3.1.5.6 2017-11-09

MICMAC Progress Update

1. Profiling update and selection of 3-4 key functions to offload to FPGA
   Makefile problem. Setup currently generates a unique makefile of same function run to run on multiple CPU's. Suggested that we concentrate on single CPU and wait for Intel OPAE framework release to help with resource distribution between multiple threads.
   https://www.altera.com/solutions/acceleration-hub/acceleration-stack.html?_ga=2.158289658.1148467054.1510237449-1361546953.1498229781&elq_cid=3114794
2. Actions for Nantes Meeting
   a. HPE: send Nallatech the kernel.
   b. Nallatech: test HPE kernel on hardware in Grenoble and look at possible optimizations.
   c. HPE: Reduce the problem to one CPU, with less images and re-profile. This will then form the new baseline for acceleration.
   d. HPE: Create 3-4 slides on MICMAC progress for Nantes F2F meeting.

3.1.5.7 2017-11-23

HPE preliminary reported on the MICMAC activity.

1 CPU core test with profiling redone, using Valgrind profiler.

The second command TAPAS is the main processing thread. The time is spent in XML parsing, so there is not much the FPGA can do with this.

The Sift Algorithm ran on each picture at the beginning. 100-300 pictures. On laptop takes 8 seconds on each picture. HPE has kernel for this. NALL will optimize and use as example for OpenCL training for ISMB.

3.1.5.8 2017-12-11

Some Potential cores of the MicMac framework to accelerate are under evaluation.

Sift ran on the first algorithm (Key point extraction). http://aishack.in/tutorials/sift-scale-invariant-feature-transform-keypoints/

ANN algorithm (Approximate Nearest Neighbor) should be evaluate for PFGA acceleration.

3.1.5.9 2017-12-20

HPE started to look at ANN algorithm.

Actions

Install OpenCL tools on server in HPE. Install old version to match BSP.

HPE to hand over sift host code and kernel for Nallatech to review and optimize.

HPE to run Micmac code with the power profiling script.

3.1.5.102017-12-21

Review IBM interconnect status

Replace FPGA card with Mellanox Card (Ethernet card does not support the full capability at this time). Infiniband does support the required RDMA (ODP) functionality.

HPE to send the model number of the Mellanox Ethernet/Inifiband card to IBM. (Edgeline 4000). M710X M510.

IBM to send HPE the details for Mellanox card.

Nallatech to update BSP of SOC card to help programmability, particularly for MICMAC porting.

3.1.5.11 2018-01-10

Progress Update from partners

Joel (IBM) making good progress with Mellanox ODP card setup and initial code working. (Server side/User Space). 65,000 to read page on Power. Updating kernel to handle page faults directly. (1-2 Weeks to kernel version working).

Currently only Power to Power. To be done to Power to HPE server.

CSI will require additional Mellanox cards to support ODP.

CNN Offload Progress

Good progress being made. Version 1 expected for end of January training.

New BSP for SOC device update

Redfish integration to taken into consideration.

3.1.5.12 2018-02-07

Update from group on progress

CNN porting. NALL explained work in progress regarding CNN and that FPGA tools have been successfully containerized.

Container migration update.

IBM: Connect X-5 ODP (On demand paging) working in user space. This required a firmware update from Mellanox. Kernel space not currently working, fix in progress. User space will be good enough for POC, so no risk to OPERA project here.

ODP is providing a small performance improvement 15-20%, but IBM suspects this is a measurement error and the actual performance is significantly better.

Actions

IBM, ISMB and NALL to collaborate on CNN paper for Sys-Store conference in Israel.

3.1.5.13 2018-03-22

ANN status update

Progress on KNN work. Code available and downloaded. HPE will profile this week for a review performance with Nallatech next week.

Nallatech will study performance of partial offloading of ANN code using the host to generate indexes (Difficult to port to FPGA). Nallatech will profile the performance of this approach for existing ANN within MICMAC. Potentially run on FPGA by next week.

Updated BSP

New BSP is complete but not delivered yet. This has increased the resource available for user designs which will improve the overall performance. This will be last update for the OPERA project.

3.1.6 WP7

In this section only the calls for the first use case, on traffic monitoring, is presented. The calls for this topic have been very frequent, due to the strict organization of the outdoor various installations. The interactions for the VDI and truck use case have been included in the discussions for WP4. The specific calls for the WP7 will be restarted in the final period of the project.

3.1.6.1 2017-09-05

1° innovation cycle

Presentation of results about detection of congestion:

- no detection with congestion 0% (11/11 detected congestion)
- 25 false detections only for way "towards Grenoble" (24 false detection for 1 event)
- no optimized optical view : confirmed by NEAVIA
- optical artefact (17/25 false alarm)

Start of the 2° innovation cycle

Presentation of the targets for the second cycle:

- Use cases:
  - Detection of congestion + wrong way vehicle
  - Detection of cycle / basic cycle counting
- Video detection specification:
  - no detection rate towards 0% : to be maintained
  - false detection rate towards 0% : to be improved
- Energy consumption
  - Below 0,5 W
  - Autonomous test site: Size & weight of energy harvesting and storage system < 1kg?

Presentation of the lesson learned (ISERE)

- Feasibility is showed
- First input data for the energy autonomous solution are available
- Improvements of the hardware integration are required
  - Mechanical and optical adjustment
- Improvement of the energy efficiency has to be investigated
  - Reducing of consumption of communication module when no communication
  - Reducing of SecSoC consumption when no vehicle
- Evaluation of the energy efficiency has to be further more investigated

- Energy consumption measurement in the field
- Evaluation of global energy efficiency

Action plan for the 2° innovation cycle

Organization of improvement action concerning the test site N°1

- Achievement of putting into operation of the test site 1:
  - Input from WP3 about Interface between SecSoC and Nucleo board:
  - Input from WP7 about transmission of data to the Moonshot server(ISERE/ISMB/NEAVIA)
  - Through the Raspberry
  - Through the LD38 firewall
- Improvement of the energy efficiency: WP3
  - Collect input from WP3 about energy efficiency possible improvement
  - Possible impact on the sizing of the energy harvesting and storage system
- Investigation about the energy efficiency : WP4/WP7
  - Energy efficiency measurement in the field (ISERE/CERTIOS/TESEO/NEAVIA/ST/ISMB)
  - Baseline for the cycle 3 (global system) (CERTIOS/ISERE)
- Status about the sizing of the energy harvesting and storage system:
  - Which size/weight of solar panel + batteries installation

Investigation about a second experimental site (ISERE+ALL)

- Which site(s)? Substitute or complementary of the site 1?
- Which use case: detection of congestion/wrong way vehicle & detection of cycle (not possible on site 1)
- Which site with an energy autonomous system?
- Which site with an ULP wireless communication system

Decision:

2 different test sites with two different prototypes for innovation cycle 2

Test site 1 on rd3 still used for detection of congestion and of wrong way vehicle: one prototype

Test site 2 to be defined used for detection of cycle and basic cycle counting: one prototype

At least the site 2 is energy autonomous and is used to measurement energy consumption in the field

Site 2 equipped with wireless

An energy autonomous installation should be sized for site 2

Under further discussion

Test site 1: supplied by grid or new reduced energy autonomous installation (+ measurement of energy consumption in the field)

Energy autonomous installation of test site 2: energy autonomous system sized in spring 2017 or more reduced energy autonomous system

Actions

- Achievement of test in site 1 related to1° innovation cycle
  - ISMB will organize a meeting with ST/NEAVIA/TESEO to achieve interface between SecSoC and Nucleo which does not operate properly
  - ISMB will send a well configured Raspberry to ISERE
  - ISERE will organize a meeting with HPE about Moonshot to install new frame
  - NEAVIA will organize a meeting with ISERE to improve the optical viewing on test site 1
- Sizing of autonomous system for 2°innovation cycle

    - ISERE will provide data to ISMB/CERTIOS: functional specifications - localization of test site
    - ISMB/CERTIOS will size again the energy harvesting and storage system. The new sizing will take account the energy efficiency improvement provided by the optimization of the operation of the Nucleo board and the SecSoC board (learned lesson from cycle 1)
- Energy efficiency measurement
    - ISERE sent a draft of specification for energy metering system (for measurement in the field) / Partners will complete it
    - ISERE answer question from CERTIOS about TMC (for global baseline for innovation cycle 3
    - CERTIOS and ISERE will have a meeting in the ISERE TMC at the end of September
- Preparation of 2° innovation cycle experimentation
    - ISERE investigate possible localization for the second test site
    - TESEO/ NEAVIA will have to discuss about the improvement of the hardware (mechanical and optical adjustment)
    - ISERE prepare an action plan for all partners

3.1.6.2 2017-09-07

Improvement of site 1

- improvement of optical view
- improvement of sensor position

3.1.6.3 2017-09-19

Test site N°1

Detection of congestion & wrong way vehicle, Location RD3- Voreppe area

- Achievement of integration of WP3 results from 1°innovation cycle
    - Hardware integration: in progress
        - Achievement of interface Nucleo/SecSoc: IN PROGRESS
        - Expectation of output from WP3: status from ST, ISMB
        - Date of implementation to be defined
        - Installation of a new Raspberry: DONE (ISMB, ISERE)
        - Supplied, installed, tested, in operation
    - Software integration : in progress
        - Installation of software « wrong way detection »: IN PROGRESS
        - Expectation of output from WP3: status from NEAVIA
        - Date of implementation to be defined
- Achievement of integration of WP5: Almost achieved
    - Installation of new version of Moonshot server: DONE (HPE, ISERE)
    - Supplied, installed, tested, in operation
    - Test of the transfer of file : file transferred, not perfectly transferred : to be investigated
    - Required complete test from SecSoC to NEAVIA server
- Integration of learned lesson
    - Required change of optical view: Required decision
        - Definition of the required optical view defined: DONE (NEAVIA, ISERE)
        - Action plan to be defined and validated: TESEO with NEAVIA, ISERE: How to do, who, when?
        - Change of position: change of sensor position in the box or change of box position
        - Change of optical magnification
    - Interaction with WP4: Blocked
        - Measurement of consumed energy impossible

- Action plan to be defined and validated: How to do, who, when?
- Installation of an energy autonomous system coupled with an energy metering system: best solution?
  (target good WP4/WP7 interaction, possible comparison SecSoc/Orlando, etc…)
- Modification of electrical installation to make possible installation of a relevant energy metering system

Test site N°2

Cycle detection & cycle detection, Location NOT DEFINED

- Supply of test site
  - Proposal of two sites with GPS coordinate : DONE (ISERE)
  - Definition of test site requirement
    - Requirement to support use case : DONE (ISERE): minimal cycle traffic during winter period
    - Requirement to support the energy autonomous OPERA system
    - Evaluation of available solar energy: ISMB : expected data
    - Sizing of energy and storage harvesting system: blocked
    - Requirement to support communication with TMC through ULP wireless link + long distance network: in progress
    - Evaluation of access point to wired network : TBD ISERE
    - Evaluation of possibility to couple Nucleo board with 3G router : TBD ISMB / TESEO
    - Requirement to support communication link dedicated to development
    - Evaluation of access point to grid: TBD ISERE
    - Proposition of solution to supply for: DONE (NEAVIA)
- Integration of WP3 results
  - Updating of specification
    - Mechanical and optical magnification adjustment ranger: expect input from NEAVIA
    - Remind of climatic condition: no freezing and no condensing system for winter period?
    - Anticipation of energy metering system
  - Final sizing of energy harvesting and storage system : blocked
  - Definition of a planning: TBD
    - New hardware design: date of supply of mechanical and electrical schematic (TESEO)
    - Validation of new hardware design: ISERE, NEAVIA, ISMB (and ST?)
    - Access to an experimental site: ISERE
    - Installation and putting into operation of hardware
    - Installation of software
    - Detection of cycle
    - Cycle counting
    - Test and evaluation
- integration of WP5 results
  - Give a network access of Moonshot server to the test site (ISERE)
- Interaction with WP4
  - Measurement of energy consumption in the field
    - Definition of specification of energy metering system : ISERE+ WP7 team : First file expected from ISERE
    - Procurement of energy metering system: Blocked (ISERE? Other?)
    - Anticipation of integration of energy metering system in hardware: TESEO

        - Installation of energy metering system: TESEO
    - Global baseline for complete use case cycle 3: start by CERTIOS
        - Organization of a meeting between CERTIOS and ISERE at ISERE TMC
        - CERTIOS send question to prepare meeting : done
        - ISERE send answer: DONE
        - CERTIOS/ ISERE fix the meeting: DONE (planned 5th October)

3.1.6.4 2017-11-08

Update of the WP7 Timeline:

- Development plan of software “detection of cycle” and “cycle counting” from WP3

Technical intervention for updating the test site 1 (optical view+ interface nucleo-SecSoc) : postponed - defining a new date and status about what will be done

Delivering of software "wrong way vehicle detection" for test in test site 1°

New test site for cycle use case

- Status about the proposal of a new hardware for cycle detection
- Status about specification for a test site (see development plan of software detection)
- New site

Coordination with development of offloading process.

3.1.6.5 2017-11-28

Review of the deadlines defined during of F2F meeting for the new installation and the improvement of the first installation.

Discussion about temporary test sites proposed by ISERE (Montbonnot, Gieres, St Egreve)

All partners agree about giving priority to the site St Egreve / ISERE need to investigate further practical issues.

The ideal scenario for all partners would be

- Installation of OPERA camera on street light just next to the cycle track
- Installation of radio receiver on the pole supporting ISERE camera (connection to wired network)
- ISERE will send further information
- NEAVIA could provide a supply system for street light, even if the street light is not supplied by LACROIX
- CERTIOS propose example of protection device against vandalism
- TESEO will participate to a physical meeting with ISERE on the site planned S48 (7th December)

Start of evaluation of congestion detection by day (not by night)

- NEAVIA confirmed that congestion detection is in operation (detection mainly in the evening) - NEAVIA will send results to ISERE
- ISERE confirmed that reference video flow is collected and will be stored by ISERE

3.1.6.6 2017-12-12

Review of deadlines defined during of F2F meeting

- Delivering of interface Nucleo-SecSoC: ASAP
- Delivering of software detection of congestion - night period : 20/12/17 - still confirmed
- Delivering of software detection of congestion: 15/02/18 still confirmed

- Delivering of HW for temporary test site 1 month after receiving information of test site by ISERE (15/01/18 for the moment) - Depend on date of selection of test site - 17th of January if decision about test site this week
- Installation of test site: 31/01/18 still confirmed
- Delivering of SW detection of cycle: 31/01/18 still confirmed
- Delivering of SW transmission of image to moonshot: 31/01/18 still confirmed
- Installation of second test site (energy autonomous): 27/04/18 still confirmed
- Delivering of SW counting of cycle: 18/05/18 still confirmed
- Delivering of FPG board: 18/05/18 still confirmed
- Delivering of SW acceleration process: 01/06/18 still confirmed

Discuss about temporary test site: two main option

- ST Egreve - on pole
    - ISERE said that installation of OPERA camera on streetlight near the cycle track is not possible
        - This streetlight is no more managed by ISERE (new law about French local authorities)
        - This streetlight is probably too small to install electrical supply system (to deliver energy during day)
    - NEAVIA said installation of OPERA camera on ISERE camera pool is not the best solution
        - Camera pole is too far and too above the cycle track
        - Camera pole does not enable to catch the expected view
    - NEAVIA said it is better to investigate the installation of the CAMERA on the streetlight located near the car park exit to test the algorithm detection of cycle Under relevant conditions
    - ISMB and TESEO confirms that a distance of a few ten of meters with a several meters difference of altitude is not a problem to test ULP radio link
    - Conclusion
        - During the visit of the 13th December, ISERE, TESEO (and NEAVIA with remote participation) will investigate the installation of a temporary test in particular with OPERA camera installed on streetlight near the car park exit, and with radio receiver installed on Camera pole
- Gieres - on VMS (Variable message signs)
    - ISERE said that it is impossible to have two locations with energy access
        - ISMB and TESEO said that to supply an energy autonomous radio receiver (with 3G router) is difficult
        - ISMB and TESEO said it is possible to test radio link with radio receiver and radio emitter both installed on the VMS, a few meter from each other's
        - CERTIOS and ISERE ask to confirm that a short enough radio link is relevant to evaluate energy consumption and consequently to size energy autonomous system
        - ISMB said that the energy consumption due to transmission of signal (high power but short duration, impacted by the distance between the emitter and the receiver) is not significant in comparison to the energy consumption due to the latency of the communication system (lower power but even longer duration, not impacted by distance between the emitter and the receiver). ISMB has to confirm.

Start of evaluation of congestion detection by day (not by night)

- Under investigation: first analysis 27-28th November
- First good detections of detection confirmed
- Probably less false detections (probably thanks to the better optical viewing)

- But irrelevant detection of the end of the afternoon congestions: probably due to start of the night
  - Confirm that to show very good results for detection of congestion will be very difficult for March, due to late test during winter period
  - Confirm requirements of more advanced software to detection congestion under night conditions

3.1.6.7 2017-12-19

Decision about temporary test site

Two main options

- Gieres on VMS
- ST Egreve on camera pole

HW design and installation is simpler and quickly in Gieres SITE, acess to St egreve site is not totally validated.

Test of software "detection of cycle" is more difficult in St Egreve, NEAVIA need an additional evaluation.

The two sites are OK for test of ULP radio link and for evaluation of energy consumption.

NEAVIA need additional test and will give the results on the 6th of January

TESEO can start a part of HW design which does not depend on type of site (new box for reconfigurable antenna, new box for camera)

ISERE reminded that the detection of cycle among car is an essential requirement for end-user as ISERE, but that for an intermediary development step, presentation of results could be focused on cycle detection rate and not on false detection rate.

3.1.6.8 2018-01-09

Decision about temporary test

Presentation of results of software test by NEAVIA

NEAVIA recommend to use

- YOLOv2 CNN architecture for Moonshot
- Tiny-Yolo CNN architecture for Embedded video platform
- COCO rather VOC as image datasets : faster and more sensitive (more over detection but treated by offloading process)
- For experimentation in February in Embedded video Platform, Tiny-YOLO combined with COCO is recommended

ST has to give information about the CNN architecture to confirm or not the use of Tiny-YOLO

NEAVIA confirms that tests can be done on Gieres sites for basic test of cycle detection

ISERE remind that this test site is to test detection of cycle, not to do an accurate evaluation of cycle counting

Decision of WP7 about test site

- Considering the results above, WP7 decide definitively to choose the test site Gières for the next experimentation in February 2018

Next Actions

- TESEO has to provide mechanical plan and electrical circuit for installation to ISERE
- ST has to provide information to NEAVIA to define the CNN architecture --> see WP3

- NEAVIA has to prepare the next software release for 31/01/18
- ISERE has to provide technical specification of power measure device to WP7/WP4.3, for completion by industrial partners
- ISERE has to analyze result of test of detection of congestion by day and by night

3.1.6.9 2018-01-23

Preparation of installation of the test site

STM as WP3 leader asks to postpone the installation from 3 to 5 weeks

STM explained that integration of the Orlando board is more complex than the SecSoC board, and required more work and test in laboratory environment (for example remote uploading of firmware cannot be done with Orlando board)

Such a delay would have a significant impact on the content of the deliverable D7.2, to be delivered at the end of March.

We would risk to be no more able to deliver test results of use case detection cycle (even basic results) for the D7.2: If the system is delivered end of February or worst beginning of March, we have Two weeks (or a few days) to start, to debug the system and to test basically the detection of cycle. It is not realistic.

So we have to take a decision about maintaining or postponing the deadline of cycle use case test and the content of D7.2

- To mobilize more (new) resources from industrial partners to maintain deadline if it is technically and economically possible.
- To drop the real condition test and to do only test in labs environment, but it should be unacceptable for WP7 and it should be critical for further steps (no results in real conditions)
- To postpone the installation and to reduce the content of deliverable to a very basic demonstration of concept: bike can be detected, first energy consumption can be measured but coordinator have to validate that it is acceptable for EC and reviewers. Even in this case, deadline has to be strictly maintained before 26th of February. Even with this deadline, it stay risked.

Isère add that

- Evaluation of use case can be adapted to the situation,
- The selected site enable relatively easy manipulation (easy access on a platform of a Variable Message Sign), we could organize intermediate intervention if required.

Congestions are correctly detected during the investigated period (02-05/01/18) including under rain and in night conditions.

There is no false detection for way to Voreppe

3.1.6.102018-01-25

Decision about the new date for the installation of test site for testing detection of cycle

Installation of test site Gieres is postponed to week 19-23 February

Delivering of SW detection of cycle (with correctly uploaded ORLANDO board) is postponed to 26 February-02 March

Delivering of interface SecSoC/Nucleo for the test site one (detection of congestion use case) is fixed at 7th February, to enable to collect additional results from test site 1

This deadline is important to collect additional results in February for the deliverable D7.2

Other topics

Visit of test site will be organized at Gieres site with WP7 members who participate to the Grenoble workshop: ST, ISMB, NEAVIA

Visit will be probably planned Tuesday 30th during the lunch break

Roberto send to ISERE additional details for installation

- Completed mechanical plan (with reconfigurable antenna) - there is no drill in the VMS infrastructure (maybe one on the box)
- Plan describing external electrical cables
- Electrical circuit plan (including plan of electrical circuit with its own circuit breakers, separated from the VMS supply circuit)
- Description of electrical devices

3.1.6.11 2018-02-06

TESEO and ISMB will come at Grenoble to install the new interface SecSoc/Nucleo in the test site 1 on the 19th of February

There will be a physical intervention both in Radio receiver site and radio emitter site.

New considerations about Gieres experimentation

- Choice about optical viewing
- Possible impact on hardware
- Possible impact on software

After discussing between ST, TESEO and NEAVIA, considering that Gieres site is used only to test cycle detection (no cycle counting)

- We keep optical viewing near the bottom of the VMS (Variable message sign) : HW is not changed
- We change angle to increase the distance between sensor and detected cycle, to increase the length of the collected view
- Angle is to be high enough to avoid negative zoom and to avoid using too high sampling rate (energy consuming)
- Angle is to be low enough to enable good cycle recognition (from side-on view)

Energy measurement system

Isère presents draft of specification.

Isère remarks that it is difficult to find a commercial energy measurement system able both to measure and to store low level of DC electrical power (tens or hundreds of mW) AND to operate in external environment : investigation are still in progress

ISERE invite to the partners to identify technical solutions.

3.1.6.12 2018-03-20

Deliverable D7.2 (review in progress)

- Point about test of radio communication - test planned next Thursday?
    - Test planned Friday 23rd of March
    - Critical issue for D7.2: all partners validated that we can no more postpone
    - Results strictly required for D7.2
- Point about wrong way detection
    - Partial results from labs test only available: contribution from NEAVIA achieved

Test site 2

- TESEO and ISMB are ready
- ST has the Orlando board, a few software issue have still to be solved
- ISERE propose to organize a "task force" (ST+ISMB+TESEO+ISERE) in the field during several days to put into operation and to solve possible bugs.

3.1.7 WP8

The activities of WP8 has been focused on the refinement of the dissemination plan, and for the organization of the communication through several main events in the period under analysis.

The consortium had regular be-weekly calls, in order to monitor the advancement of the plan.

The consortium decided through these calls to prepare some gadgets and business cards linked to the OPERA project in order to support the dissemination activities, in particular for the Hipeac main conference and other workshops during the period, until the end of the project.

The main representative of the consortium provided to the visitors theirs business cards indicating the partner's contact as well as the OPERA entry points.

Another gadget that has been provided to the guests that collaborated to the OPERA workshop was a battery pack for mobile devices as advertisement of the project.

The following paragraphs provide a list of calls, with few elements describing this process and the main topics discussed on each call.

3.1.7.1 2017-10-24

Definition of Events/workshops Roadmap

Definition of the steps for Journals and papers.

Discussion on the opportunity to realize some gadgets and business cards as support of the dissemination.

Definition of the deadlines and actions for the next WP8 deliverables.

3.1.7.2 2017-10-31

Discussed about general progression and Business cards creation.

3.1.7.3 2017-11-14

Discussed about the open points and Business cards

3.1.7.4 2017-11-28

WP8 general progresses and list of possible gadgets.

3.1.7.5 2017-12-12

WP8 general progresses and collection of the list of partners that will need a business card set.

3.1.7.6 2017-12-26

Review of the content of the deliverables D8.9, D8.10, D8.11 and D8.12 for communication, exploitation, business plan and dissemination.

3.1.7.7 2018-01-09

Discussion about the possibility to join a newly created alliance for heterogeneous systems, created by several H2020 project working on heterogeneous architectures.

Review of the ToC of the WP8 deliverables.

Preparation and review of the content of the presentations for the next Hipeac conference.

3.1.7.8 2018-01-23

Requested of contribution for deliverables 8.11 and 8.10

Completion of the review process of deliverables 8.9 and 8.12.

Discussion on the insertion of some pics of Business Cards and power banks and also about the Hipeac 2018 and the article in the Hipeac's official magazine about the last workshop of OPERA.