LOw Power Heterogeneous Architecture
for NExt Generation of SmaRt Infrastructure and Platforms
in Industrial and Societal Applications

Dissemination – Report 1

Co-funded by the Horizon 2020
Framework Programme of the European Union

DELIVERABLE NUMBER	D8.8
DELIVERABLE TITLE	Dissemination – Report 1
RESPONSIBLE AUTHOR	Idan Yaniv (Technion)

GRANT AGREEMENT N.	688386
PROJECT REF. NO	H2020- 688386
PROJECT ACRONYM	OPERA
PROJECT FULL NAME	LOw Power Heterogeneous Architecture for Next Generation of SmaRt Infrastructure and Platform in Industrial and Societal Applications
STARTING DATE (DUR.)	01/12/2015
ENDING DATE	30/11/2018
PROJECT WEBSITE	www.operaproject.eu

WORKPACKAGE N. | TITLE	WP8 | Exploitation, Impact, dissemination
WORKPACKAGE LEADER	TESEO
DELIVERABLE N. | TITLE	D8.8 | Dissemination – Report 1
RESPONSIBLE AUTHOR	Idan Yaniv (Technion)
DATE OF DELIVERY (CONTRACTUAL)	31/03/2017
DATE OF DELIVERY (SUBMITTED)	31/03/2017
VERSION | STATUS	V1 | final
NATURE	R (Report)
DISSEMINATION LEVEL	PU (Public)
AUTHORS (PARTNER)	Idan Yaniv (Technion)

VERSION	MODIFICATION(S)	DATE	AUTHOR(S)
0.1	First draft	09/01/2017	Idan Yaniv, TECHNION
1.0	Final version	31/03/2017	Idan Yaniv, TECHNION

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EXECUTIVE SUMMARY

This document is the first report of the progress made so far according to the OPERA dissemination plan. It gives a thorough account of all OPERA activities that were carried out by all partners to distribute information to various audiences within the academic and industrial communities.

Dissemination is essential for the success of the project and for the sustainability of outputs in the long term. This report (D8.8) and the upcoming updates D8.12 and D8.14 are all periodical reports of the activities aimed at fulfilling the OPERA dissemination plan, which was described in deliverable 8.4 (D8.4). Importantly, D8.4 set clear and measurable targets to monitor and report the outcomes of the project. The aforementioned reports will assess the actual status of the execution of the dissemination plan and describe what OPERA has been doing to disseminate its findings, to whom, where, and using what methods.

Even though this is just an intermediate report, the OPERA project is following well the targets that we set in D8.4, and sometimes is even exceeding the targets. We expect that, when the project will reach its final stages, more and more papers will be published, and more events and workshops will be held and organized by the industrial partners of OPERA, making us believe that thousands of scientists and engineers will be reached and learn from the OPERA project.

Finally, this report also describes a new and effective way of dissemination, which was not planned at the first stages of the OPERA project: membership in the HiPEAC community. HiPEAC is a European network of excellence on "High Performance and Embedded Architecture and Compilation". We believe that the HiPEAC membership will allow us to create important connections with other Horizon 2020 projects and disseminate the OPERA results and objectives better.

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1 DISSEMINATION PROGRESS

The OPERA Dissemination Plan, which was already submitted and accepted under Deliverable 8.4 (D8.4), defined the strategy that all the partners shall apply for publishing their OPERA research results throughout the project. D8.4 also set clear and quantitative targets to monitor and report the outcomes:

Target #1: publish 6 papers along the OPERA project in total, two per academic partner (Technion, ISMB, IBM).

Target #2: reach 2,000 people from the academic community in total. In other words, we want that at least 2,000 researchers will attend the conferences where OPERA works were presented or will read the journals where OPERA works were published.

Target #3: write at least one report for every task.

Target #4: organize 6 workshops/events along the OPERA project in total, one per industrial partner (Certios, HPE, Nallatech, Neavia, ST, Teseo).

The following sections describe the status of each of the targets, and Table 1 summarizes the progress made so far. Overall, the pace of the progress is satisfactory and sometimes even better than expected, e.g., for Targets #2, #4. Note that this document gives only an intermediate report, and so we should not expect to entirely fulfill all the targets we set in D8.4. We expect that, when the project will reach its final stages, more and more events and workshops will be held and organized by the industrial partners of OPERA.

Table 1: Progress of the dissemination targets

	Plan	Actual	Progress ratio
Target #1 (published papers)	6	3 papers	50%
Target #2 (researchers reached)	2,000	2,000	100%
Target #3 (reports per task)	1	1	100%
Target #4 (events/workshops)	6	3	50%

1.1 STATUS OF TARGET #1

The academic partners of OPERA (Technion, ISMB, and IBM) have published three papers in the first period of the project (M1—M16), as described below. These papers and posters were also published in the OPERA website, the OPERA Facebook page, and the OPERA twitter page.

1.1.1 Paper #1: Hash, Don't Cache (The Page Table)

Authors: Idan Yaniv, Dan Tsafrir.

Title: "Hash, Don't Cache (the Page Table)".

Venue: ACM SIGMETRICS International Conference on Measurement and Modeling (SIGMETRICS).

Date: June 2016.

Location: Antibes Juan-les-Pins, France.

DOI: https://doi.org/10.1145/2896377.2901456

Abstract:

Radix page tables as implemented in the x86-64 architecture incur a penalty of four memory references for address translation upon each TLB miss. These 4 references become 24 in virtualized setups, accounting for 5%–90% of the runtime and thus motivating chip vendors to incorporate page walk caches (PWCs). Counterintuitively, an ISCA 2010 paper found that radix page tables with PWCs are superior to hashed page tables, yielding up to 5x fewer DRAM accesses per page walk. We challenge this finding and show that it is the result of comparing against a suboptimal hashed implementation—that of the Itanium architecture. We show that, when carefully optimized, hashed page tables in fact outperform existing PWC-aided x86-64 hardware, shortening benchmark runtimes by 1%–27% and 6%–32% in bare-metal and virtualized setups, without resorting to PWCs. We further show that hashed page tables are inherently more scalable than radix designs and are better suited to accommodate the ever increasing memory size; their downside is that they make it more challenging to support such features as superpages.

1.1.2 Paper #2: OPERA: a Low Power Approach to the Next Generation Cloud Infrastructures

Authors: Alberto Scionti, Pietro Ruiu, Olivier Terzo, Joel Nider, Craig Petrie, Niccolo Baldoni.

Title: “OPERA: a Low Power Approach to the Next Generation Cloud Infrastructures”.

Venue: Euromicro Conference on Digital System Design (DSD).

Date: August 2016.

Location: Limassol, Cyprus.

DOI: https://doi.org/10.1109/DSD.2016.63

Abstract:

The continuous evolution of information and communication technology has led to a change in the adopted computing paradigms over time. Cloud computing is an emerging paradigm in which users, depending on their specific requirements, access to a shared pool of computing resources dynamically allocated. Cloud computing represents, with respect to Grid computing, the evolutionary step towards the implementation of a ubiquitous computing service. Such paradigm leverages on the infrastructural capabilities (compute, storage, and network) of modern data centers to provide an adequate level of computational power able to satisfy users’ requests. However, trying to continuously increase such capabilities comes at the cost of an increased energy consumption. Energy efficiency is, therefore, one of the major challenges that cloud providers must address. The OPERA project aims at bringing innovative solutions to increase the energy efficiency of cloud infrastructures, by leveraging on modular, high-density, heterogeneous and low power computing systems, which are able to cover the whole computing continuum. To this end, the project will design a highdensity server solution in which low power processors and FPGA devices will be used to accelerate cloud workloads. High-speed optical interconnections will be used to connect the proposed server with high-performance nodes, such as OpenPOWER-based machines. Cyber-Physical Systems (CPS) represents a natural extension of cloud infrastructures since they can collect and process data locally, more specifically where they were generated. OPERA aims at researching energy efficiency of such cloud endnodes by designing an ultra-low power computing system with reconfigurable radio frequency capabilities. The effectiveness of the whole platform will be demonstrated with key scenarios, specifically a road traffic monitoring application, the deployment of a virtual desktop infrastructure, and the deployment of a small data center on a truck.

1.1.3 Paper #3: Workload Management for Power Efficiency in Heterogeneous Data Centers

Authors: Pietro Ruiu, Alberto Scionti, Joel Nider, Mike Rapoport.

Title: "Workload Management for Power Efficiency in Heterogeneous Data Centers".

Venue: the 10th International Conference on Complex, Intelligent, and Software Intensive Systems (CISIS).

Date: July 2016.

Location: Fukuoka, Japan.

DOI: https://doi.org/10.1109/CISIS.2016.107

Abstract:

The cloud computing paradigm has recently emerged as a convenient solution for running different workloads on highly parallel and scalable infrastructures. One major appeal of cloud computing is its capability of abstracting hardware resources and making them easy to use. Conversely, one of the major challenges for cloud providers is the energy efficiency improvement of their infrastructures. Aimed at overcoming this challenge, heterogeneous architectures have started to become part of the standard equipment used in data centers. Despite this effort, heterogeneous systems remain difficult to program and manage, while their effectiveness has been proven only in the HPC domain. Cloud workloads are different in nature and a way to exploit heterogeneity effectively is still lacking. This paper takes a first step towards an effective use of heterogeneous architectures in cloud infrastructures. It presents an in-depth analysis of cloud workloads, highlighting where energy efficiency can be obtained. The microservices paradigm is then presented as a way of intelligently partitioning applications in such a way that different components can take advantage of the heterogeneous hardware, thus providing energy efficiency. Finally, the integration of microservices and heterogeneous architectures, as well as the challenge of managing legacy applications, is presented in the context of the OPERA project.

1.2 STATUS OF TARGET #2

According to the communication reports filled by all OPERA partners, the estimated number of researchers who were exposed to the OPERA findings and products in the first period of the project (M1—M16) is 2,000. Some of these are scientists and engineers who attended the conferences where OPERA works were presented or read the journals where OPERA works were published. Other researchers have heard about the OPERA innovative plans and products through presentations and posters delivered by the OPERA partners. We list some of these dissemination activities below:

- Technion gave an invited talk at the 4th Software Systems Summer School, which was held in the University of New South Wales (UNSW), Sydney, Australia on February 2016. The number of participants was approximately 60, most of them are academic researchers.
- Nallatech had an exhibition booth with an automated PowerPoint presentation that summarized the objectives of OPERA WP6. The presentation was given in the International Supercomputing conference (ISC), which was held in Frankfurt, Germany on 20—23 June 2016. According to Nallatech estimations, there were ~3,000 attendees in total at the event.
- Nallatech also had an exhibition booth at the ACM/IEEE Supercomputing conference (SC), which was held in Salt Lake City, US on November 13—18 2016. Nallatech estimated that ~3,000 attended the event.

- Nallatech presented an overview of its FPGA technology and its participation in OPERA project in the Computing Insight event, which was held in Manchester, UK on December 14—15 2016. About 300 attended this academic-orientated conference and exhibition.

1.3 STATUS OF TARGET #3

In the original OPERA grant agreement, all OPERA tasks committed to deliver one document that summarizes the work under this task. According to the feedback from the reviewers in the first review (M9), most of the tasks further committed to one or more intermediate reports and deliverables, thus enhancing and promising the achievement of Target #3. Moreover, all OPERA deliverables so far were delivered on time.

1.4 STATUS OF TARGET #4

During the first months of the OPERA project, there were three workshops/events organized by HPE and Nallatech, in which they presented OPERA products:

1.4.1 HPE OSL-TES

Nallatech presented an overview of FPGA technology that included a section on OPERA work package 6 (WP6), where Nallatech is working with HPE and IBM to integrate FPGA/SoC technology into the HPE Edgeline server to create a next generation Small Form Factor Data Center platform, and Nallatech explained how they are using OpenCL to improve the programming model. Nallatech estimated that there were 20 attendees in the presentation.

The event was hosted under the HPE OSL-TES [1] event (full name: 8th HPE High Performance Computing Open Source & Linux Technical Excellence Symposium for HPE EMEA EG Presales & HPE Channel Partners). The event was held in Grenoble, France in March 14—18, 2016.

1.4.2 HP-CAST 26 + HP-CAST 27

Nallatech participated in two HP-CAST events and presented an overview of FPGA technology that included a section on OPERA WP6 where Nallatech is working with HPE and IBM to integrate FPGA/SoC technology into the HPE Edgeline server to create a next generation Small Form Factor Data Center platform. They also explained how the OPERA project is using the OpenCL to improve the programming model. There were ~30 attendees in the presentation.

The HP-CAST event (full name: the worldwide conference of the High Performance Consortium for Advanced Scientific and Technical computing users group) is a consortium that works to increase the capabilities of Hewlett Packard Enterprise solutions for large-scale, scientific and technical computing. HP-CAST provides guidance to Hewlett Packard Enterprise on the essential development and support issues for such systems. HP-CAST meetings typically include corporate briefings and presentations by HPE executives and technical staff (under NDA), and discussions of customer issues related to high-performance technical computing.

The HP-CAST 26 event was held in Frankfurt, Germany on 16—19 June 2016.

The HP-CAST 27 event was held in Salt Lake City, US on 11—13 November 2016.

2 HIPEAC MEMBERSHIP

HiPEAC is a European network of excellence on "High Performance and Embedded Architecture and Compilation". It is one of the most active research community in the computer architecture field, promoting several events and allowing EU projects to disseminate results and objectives.

Since few years, the HiPEAC network allows EU funded projects to become stakeholder members to better represent the project in front of the community and allows to share results, ideas and common objectives. The OPERA project is one of the stakeholders of the network [2] since November 2016, which enables to disseminate and spread the OPERA results effectively. There is also a HiPEAC conference organized every year, which is a good venue to meet other groups, and to search partners for collaborations.

The HiPEAC membership was proven to be very beneficial and created important connections with other Horizon 2020 projects dealing with problems related to the OPERA use cases. For example, the OPERA project have been invited to be part of a workshop organized by University of Bielefeld, which is a partner in the M2DC project consortium. The workshop will be held in the next International Supercomputing conference (ISC) 2017. Another example is that ISMB and other OPERA partners are organizing a thematic session in the next HiPEAC Computing System Week (CSW), covering “heterogeneity and low power system in next generation datacentres”, and inviting the following Horizon 2020 projects: M2DC, VINEYARD, DREDBOX, ECOSCALE.

During the HiPEAC 2016 conference (held on January 18-20, 2016, in Prague, Czech Republic) ISMB also presented a poster [3] and estimated that 30 visitors had a look at the poster during the poster session.

3 REFERENCES

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[4] OPERA Consortium, “D8.1. Communication Strategy,” OPERA, 2016.